



## 5.0 A Throttle Control H-bridge

The 33931 is a monolithic H-bridge Power IC in a robust thermally enhanced package. It is designed primarily for automotive electronic throttle control, but is applicable to any low-voltage DC servo motor control application within the current and voltage limits stated in this specification.

The 33931 H-bridge is able to control inductive loads with currents up to 5.0 A peak. RMS current capability is subject to the degree of heatsinking provided to the device package. Internal peak-current limiting (regulation) is activated at load currents above  $6.5 \text{ A} \pm 1.5 \text{ A}$ . Output loads can be pulse width modulated (PWM-ed) at frequencies up to 11 kHz. A load current feedback feature provides a proportional (0.24% of the load current) current output suitable for monitoring by a microcontroller's A/D input. A Status Flag output reports under-voltage, over-current, and over-temperature fault conditions.

Two independent inputs provide polarity control of two half-bridge totem-pole outputs. The disable inputs are provided to force the H-bridge outputs to tri-state (high-impedance off-state).

### Features

- 8.0 V to 28 V continuous operation (transient operation from 5.0 V to 40 V)
- 235 mΩ maximum  $R_{DS(ON)}$  @  $T_J=150^\circ\text{C}$  (each H-bridge MOSFET)
- 3.0 V and 5.0 V TTL / CMOS logic compatible inputs
- Over-current limiting (regulation) via internal constant-off-time PWM
- Output short-circuit protection (short to VPWR or GND)
- Temperature-dependant current-limit threshold reduction
- All inputs have an internal source/sink to define the default (floating input) states
- Sleep mode with current draw  $< 50 \mu\text{A}$  (each half with inputs floating or set to match default logic states)

**33931**

**THROTTLE CONTROL H-BRIDGE**



ORDERING INFORMATION		
Device	Temperature Range ( $T_A$ )	Package
MC33931VW/R2	-40°C to 125°C	44 HSOP

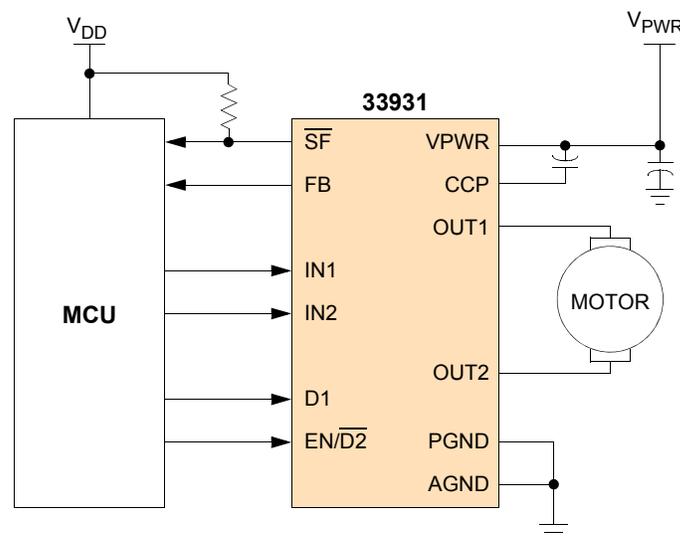


Figure 1. MC33931 Simplified Application Diagram

\* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

### INTERNAL BLOCK DIAGRAM

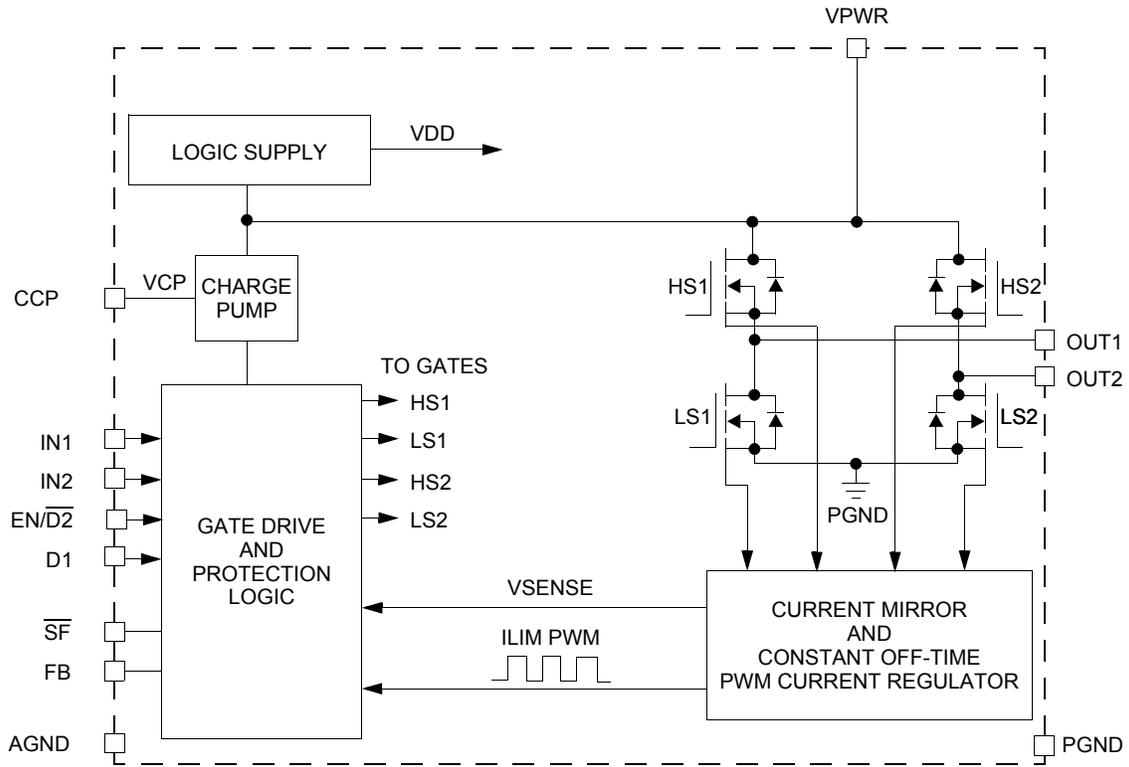


Figure 2. 33931 Simplified Internal Block Diagram

## PIN CONNECTIONS

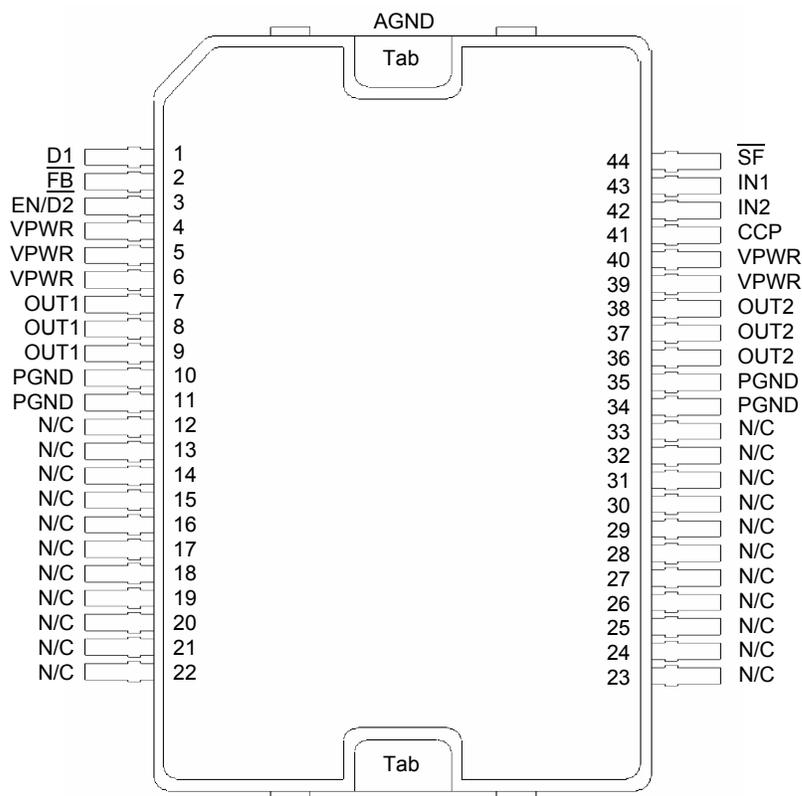


Figure 3. 33931 Pin Connections

Table 1. 33931 Pin Definitions

A functional description of each pin can be found in the Functional Description section beginning on <a href="#">page 11</a> .				
Pin	Pin Name	Pin Function	Formal Name	Definition
1	D1	Logic Input	Disable Input 1 (Active High)	When D1 is logic HIGH, both OUT1 and OUT2 are tri-stated. Schmitt trigger input with ~80 $\mu$ A source so default condition = disabled.
2	FB	Analog Output	Feedback	The load current feedback output provides ground referenced 0.24% of the high side output current. (Tie to GND through a resistor if not used.)
3	EN/D2	Logic Input	Enable Input	When EN/D2 is logic HIGH the H-bridge is operational. When EN/D2 is logic LOW, the H-bridge outputs are tri-stated and placed in Sleep mode. (logic input with ~80 $\mu$ A sink so default condition = Sleep mode.)
4-6,40,39	VPWR	Power Input	Positive Power Supply	These pins must be connected together physically as close as possible and directly soldered down to a wide, thick, low resistance supply plane on the PCB.
7-9	OUT1	Power Output	H-bridge Output 1	Source of high side MOSFET1 and drain of low side MOSFET1.
10,11,34,35	PGND	Power Ground	Power Ground	High-current power ground pins must be connected together physically as close as possible and directly soldered down to a wide, thick, low resistance ground plane on the PCB.
36-38	OUT2	Power Output	H-bridge Output 2	Source of high side MOSFET2 and drain of low side MOSFET2.

**Table 1. 33931 Pin Definitions (continued)**

A functional description of each pin can be found in the Functional Description section beginning on [page 11](#).

Pin	Pin Name	Pin Function	Formal Name	Definition
41	CCP	Analog Output	Charge Pump Capacitor	External reservoir capacitor connection for the internal charge pump; connected to VPWR. Allowable values are 30 nF to 100 nF. <b>Note:</b> This capacitor is required for the proper performance of the device.
42	IN2	Logic Input	Input 2	Logic input control of OUT2; e.g., when IN2 is logic HIGH, OUT2 is set to VPWR, and when IN2 is logic LOW, OUT2 is set to PGND. (Schmitt trigger Input with ~80 $\mu$ A source so default condition = OUT2 HIGH.)
43	IN1	Logic Input	Input 1	Logic input control of OUT1; e.g., when IN1 is logic HIGH, OUT1 is set to VPWR, and when IN1 is logic LOW, OUT1 is set to PGND. (Schmitt trigger Input with ~80 $\mu$ A source so default condition = OUT1 HIGH.)
44	$\overline{\text{SF}}$	Logic Output - Open Drain	Status Flag (Active Low)	Open drain active LOW Status Flag output (requires an external pull-up resistor to $V_{DD}$ . Maximum permissible load current < 0.5 mA. Maximum $V_{CEsat}$ < 0.4 V @ 0.3 mA. Maximum permissible pull-up voltage < 7.0 V.)
TAB	AGND	Analog Ground	Analog Signal Ground	The low-current analog signal ground must be connected to PGND via low-impedance path (<10 m $\Omega$ , 0 Hz to 20 kHz). Exposed TAB is also the main heatsinking path for the device.
12-33	N/C	None	No Connect	Pin is not used

## ELECTRICAL CHARACTERISTICS

## MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device. These parameters are not production tested.

Ratings	Symbol	Value	Unit
<b>ELECTRICAL RATINGS</b>			
Power Supply Voltage			V
Normal Operation (Steady-state)	$V_{PWR(SS)}$	-0.3 to 28	
Transient Over-voltage <sup>(1)</sup>	$V_{PWR(T)}$	-0.3 to 40	
Logic Input Voltage <sup>(2)</sup>	$V_{IN}$	-0.3 to 7.0	V
$\overline{SF}$ Output <sup>(3)</sup>	$V_{\overline{SF}}$	-0.3 to 7.0	V
Continuous Output Current <sup>(4)</sup>	$I_{OUT(CONT)}$	5.0	A
ESD Voltage <sup>(5)</sup>			V
Human Body Model	$V_{ESD1}$	±2000	
Machine Model	$V_{ESD2}$	±200	
Charge Device Model			
Corner Pins (1,22,23,44)		±750	
All Other Pins		±500	
<b>THERMAL RATINGS</b>			
Storage Temperature	$T_{STG}$	-65 to 150	°C
Operating Temperature <sup>(6)</sup>			°C
Ambient	$T_A$	-40 to 125	
Junction	$T_J$	-40 to 150	
Peak Package Reflow Temperature During Reflow <sup>(7),(8)</sup>	$T_{PPRT}$	Note 8	°C
Approximate Junction-to-Case Thermal Resistance <sup>(9)</sup>	$R_{\theta JC}$	<1.0	°C/W

## Notes

- Device will survive repetitive transient over-voltage conditions for durations not to exceed 500 ms @ duty cycle not to exceed 10%. External protection is required to prevent device damage in case of a reverse battery condition.
- Exceeding the maximum input voltage on IN1, IN2, EN/ $\overline{D2}$  or D1 may cause a malfunction or permanent damage to the device.
- Exceeding the pull-up resistor voltage on the open drain  $\overline{SF}$  pin may cause permanent damage to the device.
- Continuous output current capability is dependent on sufficient package heatsinking to keep junction temperature  $\leq 150^\circ\text{C}$ .
- ESD testing is performed in accordance with the Human Body Model ( $C_{ZAP} = 100 \text{ pF}$ ,  $R_{ZAP} = 1500 \Omega$ ), Machine Model ( $C_{ZAP} = 200 \text{ pF}$ ,  $R_{ZAP} = 0 \Omega$ ), and the Charge Device Model (CDM), Robotic ( $C_{ZAP} = 4.0 \text{ pF}$ ).
- The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking provided. Brief non-repetitive excursions of junction temperature above  $150^\circ\text{C}$  can be tolerated, provided the duration does not exceed 30 seconds maximum. (Non-repetitive events are defined as not occurring more than once in 24 hours.)
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx)], and review parametrics.
- Exposed heatsink pad plus the power and ground pins comprise the main heat conduction paths. The actual  $R_{\theta JB}$  (junction-to-PC board) values will vary depending on solder thickness and composition and copper trace thickness and area. Maximum current at maximum die temperature represents ~16 W of conduction loss heating in the diagonal pair of output MOSFETs. Therefore, the  $R_{\theta JA}$  must be  $<5.0^\circ\text{C/W}$  for maximum current at  $70^\circ\text{C}$  ambient. Module thermal design must be planned accordingly.

**STATIC ELECTRICAL CHARACTERISTICS**

**Table 3. Static Electrical Characteristics**

Characteristics noted under conditions  $8.0\text{ V} \leq V_{PWR} \leq 28\text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>POWER INPUTS (VPWR)</b>					
Operating Voltage Range <sup>(10)</sup>					V
Steady-state	$V_{PWR(SS)}$	8.0	–	28	
Transient ( $t < 500\text{ ms}$ ) <sup>(11)</sup>	$V_{PWR(t)}$	–	–	40	
Quasi-Functional ( $R_{DS(ON)}$ May Increase by 50%)	$V_{PWR(QF)}$	5.0	–	8.0	
Sleep State Supply Current <sup>(12)</sup>	$I_{PWR(SLEEP)}$				$\mu\text{A}$
$\text{EN}/\overline{\text{D2}} = \text{Logic [0]}, \text{IN1}, \text{IN2}, \text{D1} = \text{Logic [1]}, \text{and } I_{OUT} = 0\text{ A}$		–	–	50	
Standby Supply Current (Part Enabled)	$I_{PWR(STANDBY)}$				mA
$I_{OUT} = 0\text{ A}, V_{EN} = 5.0\text{ V}$		–	–	20	
Under-voltage Lockout Thresholds					
$V_{PWR(\text{falling})}$	$V_{UVLO(ACTIVE)}$	4.15	–	–	V
$V_{PWR(\text{rising})}$	$V_{UVLO(INACTIVE)}$	–	–	5.0	V
Hysteresis	$V_{UVLO(HYS)}$	150	200	350	mV
<b>CHARGE PUMP</b>					
Charge Pump Voltage (CP Capacitor = 33 nF), No PWM	$V_{CP} - V_{PWR}$				V
$V_{PWR} = 5.0\text{ V}$		3.5	–	–	
$V_{PWR} = 28\text{ V}$		–	–	12	
Charge Pump Voltage (CP Capacitor = 33 nF), PWM = 11 kHz,	$V_{CP} - V_{PWR}$				V
$V_{PWR} = 5.0\text{ V}$		3.5	–	–	
$V_{PWR} = 28\text{ V}$		–	–	12	
<b>CONTROL INPUTS</b>					
Operating Input Voltage (IN1, IN2, D1, $\text{EN}/\overline{\text{D2}}$ )	$V_I$	–	–	5.5	V
Input Voltage (IN1, IN2, D1, $\text{EN}/\overline{\text{D2}}$ )					
Logic Threshold HIGH	$V_{IH}$	2.0	–	–	V
Logic Threshold LOW	$V_{IL}$	–	–	1.0	V
Hysteresis	$V_{HYS}$	250	400	–	mV
Logic Input Currents, $V_{PWR} = 8.0\text{ V}$	$I_{IN}$				$\mu\text{A}$
Input $\text{EN}/\overline{\text{D2}}$ (internal pull-downs), $V_{IH} = 5.0\text{ V}$		20	80	200	
Inputs IN1, IN2, D1 (internal pull-ups), $V_{IL} = 0\text{ V}$		-200	-80	-20	

Notes

- Device specifications are characterized over the range of  $8.0\text{ V} \leq V_{PWR} \leq 28\text{ V}$ . Continuous operation above 28 V may degrade device reliability. Device is operational down to 5.0 V, but below 8.0 V the output resistance may increase by 50 percent.
- Device will survive the transient over-voltage indicated for a maximum duration of 500 ms. Transient not to be repeated more than once every 10 seconds.
- $I_{PWR(SLEEP)}$  is with Sleep Mode activated and  $\text{EN}/\overline{\text{D2}} = \text{logic [0]}$ , and IN1, IN2, D1 = logic [1] or with these inputs left floating.

**Table 3. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $8.0\text{ V} \leq V_{PWR} \leq 28\text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>POWER OUTPUTS OUT1, OUT2</b>					
Output-ON Resistance <sup>(14)</sup> , $I_{LOAD} = 3.0\text{ A}$ $V_{PWR} = 8.0\text{ V}$ , $T_J = 25^\circ\text{C}$ $V_{PWR} = 8.0\text{ V}$ , $T_J = 150^\circ\text{C}$ $V_{PWR} = 5.0\text{ V}$ , $T_J = 150^\circ\text{C}$	$R_{DS(ON)}$	–	120	–	m $\Omega$
Output Current Regulation Threshold $T_J < T_{FB}$ $T_J \geq T_{FB}$ (Foldback Region - see Figure 9 and Figure 11) <sup>(13)</sup>	$I_{LIM}$	5.2	6.5	8.0	A
High Side Short Circuit Detection Threshold (Short Circuit to Ground) <sup>(13)</sup>	$I_{SCH}$	11	13	16	A
Low Side Short Circuit Detection Threshold (Short Circuit to $V_{PWR}$ ) <sup>(13)</sup>	$I_{SCL}$	9.0	11	14	A
Output Leakage Current <sup>(15)</sup> , Outputs off, $V_{PWR} = 28\text{ V}$ $V_{OUT} = V_{PWR}$ $V_{OUT} = \text{Ground}$	$I_{OUTLEAK}$	–	–	100	$\mu\text{A}$
Output MOSFET Body Diode Forward Voltage Drop, $I_{OUT} = 3.0\text{ A}$	$V_F$	–	–	2.0	V
Over-temperature Shutdown <sup>(13)</sup> Thermal Limit @ $T_J$ Hysteresis @ $T_J$	$T_{LIM}$ $T_{HYS}$	175	–	200	$^\circ\text{C}$
Current Foldback at $T_J$ <sup>(13)</sup>	$T_{FB}$	165	–	185	$^\circ\text{C}$
Current Foldback to Thermal Shutdown Separation <sup>(13)</sup>	$T_{SEP}$	10	–	15	$^\circ\text{C}$

**HIGH SIDE CURRENT SENSE FEEDBACK**

Feedback Current (pin FB sourcing current) <sup>(16)</sup> $I_{OUT} = 0\text{ mA}$ $I_{OUT} = 300\text{ mA}$ $I_{OUT} = 500\text{ mA}$ $I_{OUT} = 1.5\text{ A}$ $I_{OUT} = 3.0\text{ A}$ $I_{OUT} = 6.0\text{ A}$	$I_{FB}$	0.0	–	50	$\mu\text{A}$
		0.0	270	750	$\mu\text{A}$
		0.35	0.775	1.56	mA
		2.86	3.57	4.28	mA
		5.71	7.14	8.57	mA
		11.43	14.29	17.15	mA

**STATUS FLAG<sup>(17)</sup>**

Status Flag Leakage Current <sup>(18)</sup> $V_{SF} = 5.0\text{ V}$	$I_{SFLEAK}$	–	–	5.0	$\mu\text{A}$
Status Flag SET Voltage <sup>(19)</sup> $I_{SF} = 300\text{ }\mu\text{A}$	$V_{SFLOW}$	–	–	0.4	V

Notes

- This parameter is Guaranteed By Design.
- Output-ON resistance as measured from output to  $V_{PWR}$  and from output to GND.
- Outputs switched OFF via D1 or  $\overline{\text{EN/D2}}$ .
- Accuracy is better than 20% from 0.5 A to 6.0 A. Recommended terminating resistor value:  $R_{FB} = 270\text{ }\Omega$ .
- Status Flag output is an open drain output requiring a pull-up resistor to logic  $V_{DD}$ .
- Status Flag Leakage Current is measured with Status Flag HIGH and *not* SET.
- Status Flag Set Voltage measured with Status Flag LOW and SET with  $I_{SF} = 300\text{ }\mu\text{A}$ . Maximum allowable sink current from this pin is  $< 500\text{ }\mu\text{A}$ . Maximum allowable pull-up voltage  $< 7.0\text{ V}$ .

**DYNAMIC ELECTRICAL CHARACTERISTICS**

**Table 4. Dynamic Electrical Characteristics**

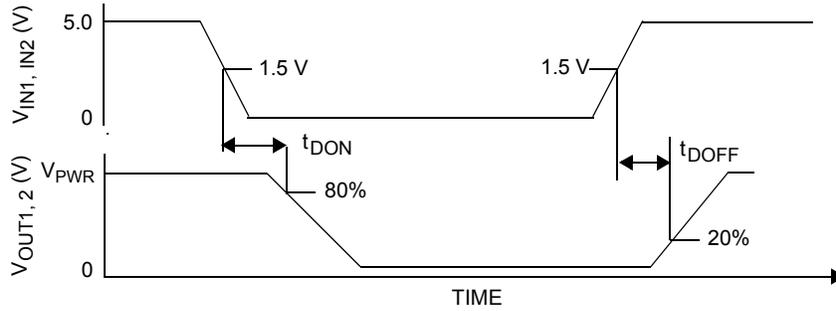
Characteristics noted under conditions  $8.0\text{ V} \leq V_{PWR} \leq 28\text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>TIMING CHARACTERISTICS</b>					
PWM Frequency <sup>(20)</sup>	$f_{PWM}$	–	–	11	kHz
Maximum Switching Frequency During Current Limit Regulation <sup>(21)</sup>	$f_{MAX}$	–	–	20	kHz
Output ON Delay <sup>(22)</sup> $V_{PWR} = 14\text{ V}$	$t_{DON}$	–	–	18	$\mu\text{s}$
Output OFF Delay <sup>(22)</sup> $V_{PWR} = 14\text{ V}$	$t_{DOFF}$	–	–	12	$\mu\text{s}$
$I_{LIM}$ Output Constant-OFF Time <sup>(23)</sup>	$t_A$	15	20.5	32	$\mu\text{s}$
$I_{LIM}$ Blanking Time <sup>(24)</sup>	$t_B$	12	16.5	27	$\mu\text{s}$
Disable Delay Time <sup>(25)</sup>	$t_{DDISABLE}$	–	–	8.0	$\mu\text{s}$
Output Rise and Fall Time <sup>(26)</sup>	$t_F, t_R$	1.5	3.0	8.0	$\mu\text{s}$
Short-circuit/Over-temperature Turn-OFF (Latch-OFF) Time <sup>(27),(28)</sup>	$t_{FAULT}$	–	–	8.0	$\mu\text{s}$
Power-ON Delay Time <sup>(28)</sup>	$t_{POD}$	–	1.0	5.0	ms
Output MOSFET Body Diode Reverse Recovery Time <sup>(28)</sup>	$t_{RR}$	75	100	150	ns
Charge Pump Operating Frequency <sup>(28)</sup>	$f_{CP}$	–	7.0	–	MHz

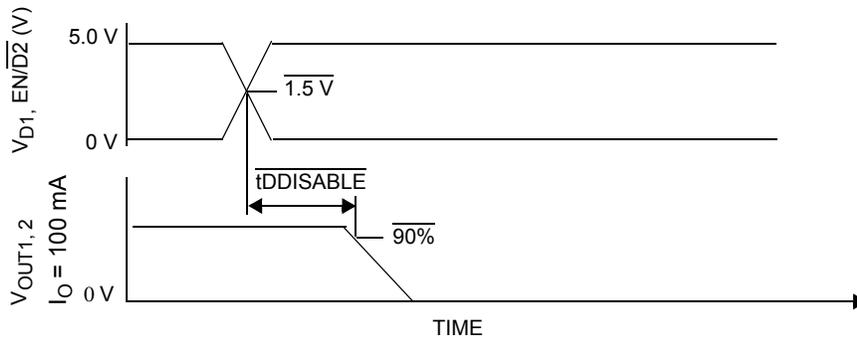
Notes

20. The maximum PWM frequency should be limited to frequencies < 11 kHz in order to allow the internal high side driver circuitry time to fully enhance the high side MOSFETs.
21. The internal current limit circuitry produces a constant-OFF-time Pulse Width Modulation of the output current. The output load's inductance, capacitance, and resistance characteristics affect the total switching period (OFF-time + ON-time), and thus the PWM frequency during current limit.
22. \* Output Delay is the time duration from 1.5 V on the IN1 or IN2 input signal to the 20% or 80% point (dependent on the transition direction) of the OUT1 or OUT2 signal. If the output is transitioning HIGH-to-LOW, the delay is from 1.5 V on the input signal to the 80% point of the output response signal. If the output is transitioning LOW-to-HIGH, the delay is from 1.5 V on the input signal to the 20% point of the output response signal. See [Figure 4](#), page 9.
23. The time during which the internal constant-OFF time PWM current regulation circuit has tri-stated the output bridge.
24. The time during which the current regulation threshold is ignored so that the short-circuit detection threshold comparators may have time to act.
25. \* Disable Delay Time measurement is defined in [Figure 5](#), page 9.
26. Rise Time is from the 10% to the 90% level and Fall Time is from the 90% to the 10% level of the output signal with  $V_{PWR} = 14\text{ V}$ ,  $R_{LOAD} = 3.0\text{ ohm}$ . See [Figure 6](#), page 9.
27. Load currents ramping up to the current regulation threshold become limited at the  $I_{LIM}$  value (see [Figure 7](#)). The short-circuit currents possess a di/dt that ramps up to the  $I_{SCH}$  or  $I_{SCL}$  threshold during the  $I_{LIM}$  blanking time, registering as a short-circuit event detection and causing the shutdown circuitry to force the output into an immediate tri-state latch-OFF (see [Figure 8](#)). Operation in Current Limit mode may cause junction temperatures to rise. Junction temperatures above  $\sim 160^\circ\text{C}$  will cause the output current limit threshold to “fold back”, or decrease, until  $\sim 175^\circ\text{C}$  is reached, after which the  $T_{LIM}$  thermal latch-OFF will occur. Permissible operation within this fold back region is limited to non-repetitive transient events of duration not to exceed 30 seconds (see [Figure 9](#)).
28. Parameter is Guaranteed By Design.

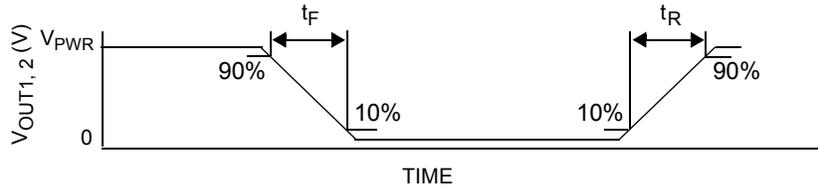
**TIMING DIAGRAMS**



**Figure 4. Output Delay Time**

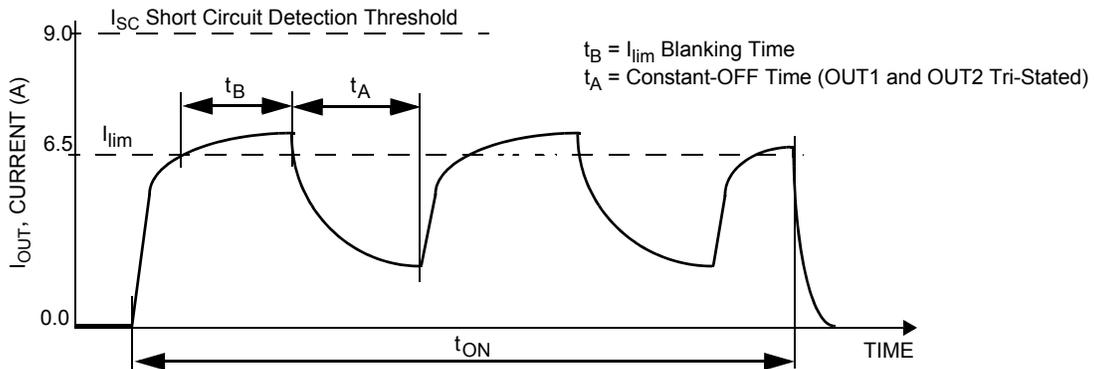


**Figure 5. Disable Delay Time**



**Figure 6. Output Switching Time**

**Overload Condition**



**Figure 7. Current Limit Blanking Time and Constant-OFF Time**

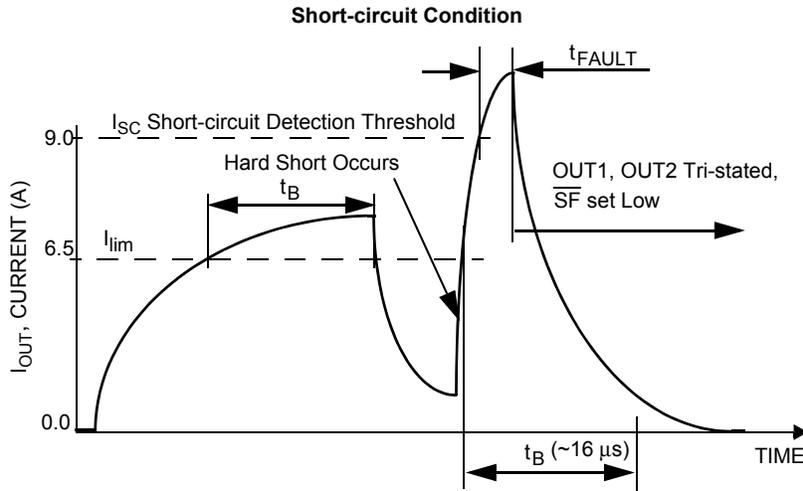


Figure 8. Short-circuit Detection Turn-OFF Time  $t_{FAULT}$

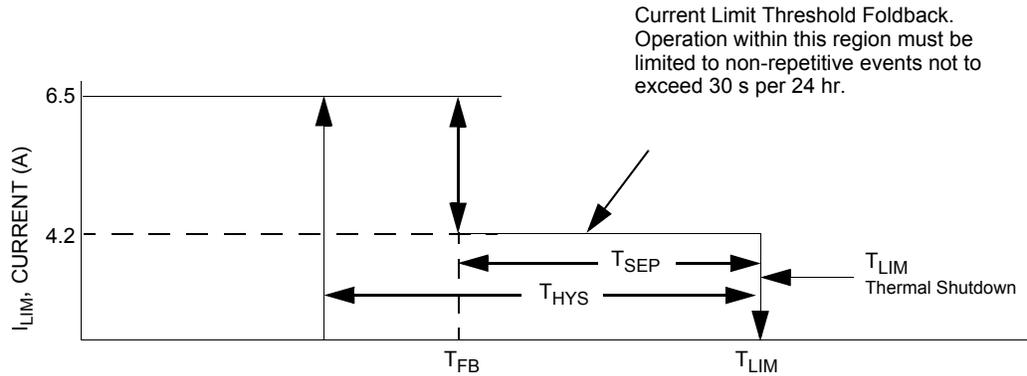


Figure 9. Output Current Limiting Foldback Region

## FUNCTIONAL DESCRIPTION

### INTRODUCTION

Numerous protection and operational features (speed, torque, direction, dynamic braking, PWM control, and closed-loop control) make the 33931 a very attractive, cost-effective solution for controlling a broad range of small DC motors. The 33931 outputs are capable of supporting peak DC load currents of up to 5.0 A from a 28 V  $V_{PWR}$  source. An internal charge pump and gate drive circuitry are provided that can support external PWM frequencies up to 11 kHz.

The 33931 has an analog feedback (current mirror) output pin (the FB pin) that provides a constant-current source ratioed to the active high side MOSFETs' current. This can be used to provide "real time" monitoring of output current to facilitate closed-loop operation for motor speed/torque control, or for the detection of open load conditions.

Two independent inputs, IN1 and IN2, provide control of the two totem-pole half-bridge outputs. Two independent disable inputs, D1 and EN/D2, provide the means to force the H-bridge outputs to a high-impedance state (all H-bridge switches OFF). The EN/D2 pin also controls an enable

function that allows the IC to be placed in a power-conserving Sleep mode.

The 33931 has output current limiting (via constant OFF-time PWM current regulation), output short-circuit detection with latch-OFF, and over-temperature detection with latch-OFF. Once the device is latched-OFF due to a fault condition, either of the Disable inputs (D1 or EN/D2), or  $V_{PWR}$  must be "toggled" to clear the status flag.

Current limiting (Load Current Regulation) is accomplished by a constant-OFF time PWM method using current limit threshold triggering. The current limiting scheme is unique in that it incorporates a junction temperature-dependent current limit threshold. This means that the current limit threshold is "reduced to around 4.2 A" as the junction temperature increases above 160°C. When the temperature is above 175°C, over-temperature shutdown (latch-OFF) will occur. This combination of features allows the device to continue operating for short periods of time (<30 seconds) with unexpected loads, while still retaining adequate protection for both the device and the load.

### FUNCTIONAL PIN DESCRIPTION

#### POWER GROUND AND ANALOG GROUND (PGND AND AGND)

The power and analog ground pins should be connected together with a very low-impedance connection.

#### POSITIVE POWER SUPPLY (VPWR)

VPWR pins are the power supply inputs to the device. All VPWR pins must be connected together on the printed circuit board with as short as possible traces, offering as low an impedance as possible between pins.

#### STATUS FLAG ( $\overline{SF}$ )

This pin is the device fault status output. This output is an active LOW open drain structure requiring a pull-up resistor to  $V_{DD}$ . The maximum  $V_{DD}$  is <7.0 V. Refer to [Table 5, Truth Table](#), page 15 for the SF Output status definition.

#### INPUT 1,2 AND DISABLE INPUT 1 (IN1, IN2, AND D1)

These pins are input control pins used to control the outputs. These pins are 3.0 V/5.0 V CMOS-compatible inputs with hysteresis. IN1 and IN2 independently control OUT1 and OUT2, respectively. D1 input is used to tri-state disable the H-bridge outputs.

When D1 is SET (D1 = logic HIGH) in the disable state, outputs OUT1 and OUT2 are both tri-state disabled; however, the rest of the device circuitry is fully operational and the

supply  $I_{PWR(STANDBY)}$  current is reduced to a few mA. Refer to [Table 3, Static Electrical Characteristics](#), page 6.

#### H-BRIDGE OUTPUT (OUT1, OUT2)

These pins are the outputs of the H-bridge with integrated free-wheeling diodes. The bridge output is controlled using the IN1, IN2, D1, and EN/D2 inputs. The outputs have PWM current limiting above the  $I_{LIM}$  threshold. The outputs also have thermal shutdown (tri-state latch-OFF) with hysteresis as well as short circuit latch-OFF protection.

A disable timer (time  $t_b$ ) is incorporated to distinguish between load currents that are higher than the  $I_{LIM}$  threshold and short circuit currents. This timer is activated at each output transition.

#### CHARGE PUMP CAPACITOR (CCP)

This pin is the charge pump output pin and connection for the external charge pump reservoir capacitor. The allowable value is from 30 nF to 100 nF. This capacitor must be connected from the CCP pin to the VPWR pin. The device cannot operate properly without the external reservoir capacitor.

#### ENABLE INPUT/DISABLE INPUT 2 (EN/D2)

The EN/D2 pin performs the same function as D1 pin, when it goes to a logic LOW the outputs are immediately tri-stated. It is also used to place the device in a Sleep mode so as to consume very low currents. When the EN/D2 pin voltage is a logic LOW state, the device is in the Sleep mode.

The device is enabled and fully operational when the EN pin voltage is logic HIGH. An internal pull-down resistor maintains the device in Sleep mode in the event EN is driven through a high-impedance I/O or an unpowered microcontroller, or the EN/D2 input becomes disconnected.

### **FEEDBACK (FB)**

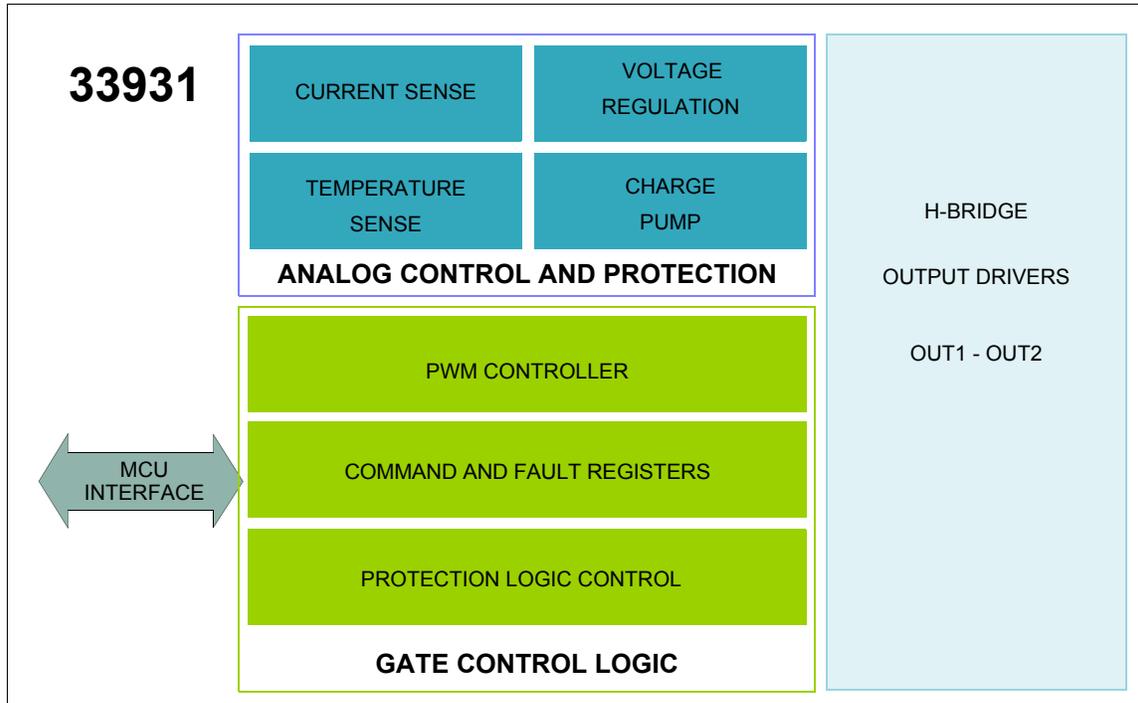
The 33931 has a feedback output (FB) for “real time” monitoring of H-bridge high side output currents to facilitate closed-loop operation for motor speed and torque control.

The FB pin provides current sensing feedback of the H-bridge high side drivers. When running in the forward or reverse direction, a ground-referenced 0.24% of load current

is output to this pin. Through the use of an external resistor to ground, the proportional feedback current can be converted to a proportional voltage equivalent and the controlling microcontroller can “read” the current proportional voltage with its analog-to-digital converter (ADC). This is intended to provide the user with only first-order motor current feedback for motor torque control. The resistance range for the linear operation of the FB pin is  $100 \Omega < R_{FB} < 300 \Omega$ .

If PWM-ing is implemented using the disable pin input (only D1), a small filter capacitor ( $\sim 1.0 \mu\text{F}$ ) may be required in parallel with the  $R_{FB}$  resistor to ground for spike suppression.

**FUNCTIONAL INTERNAL BLOCK DESCRIPTION**



**Figure 10. Functional Internal Block Diagram**

**ANALOG CONTROL AND PROTECTION CIRCUITRY:**

An on-chip voltage regulator supplies the internal logic. The charge pump provides gate drive for the H-bridge MOSFETs. The Current and Temperature sense circuitry provides detection and protection for the output drivers. Output under-voltage protection shuts down the MOSFETS.

**GATE CONTROL LOGIC:**

The 33931 is a monolithic H-bridge Power IC designed primarily for any low-voltage DC servo motor control application within the current and voltage limits stated for the device. Two independent inputs provide polarity control of

two half-bridge totem-pole outputs. Two independent disable inputs are provided to force the H-bridge outputs to tri-state (high-impedance off-state).

**H-BRIDGE OUTPUT DRIVERS: OUT1 AND OUT2**

The H-bridge is the power output stage. The current flow from OUT1 to OUT2 is reversible and under full control of the user by way of the Input Control Logic. The output stage is designed to produce full load control under all system conditions. All protective and control features are integrated into the Control and Protection blocks. The sensors for current and temperature are integrated directly into the output MOSFET for maximum accuracy and dependability.

## FUNCTIONAL DEVICE OPERATION

### OPERATIONAL MODES

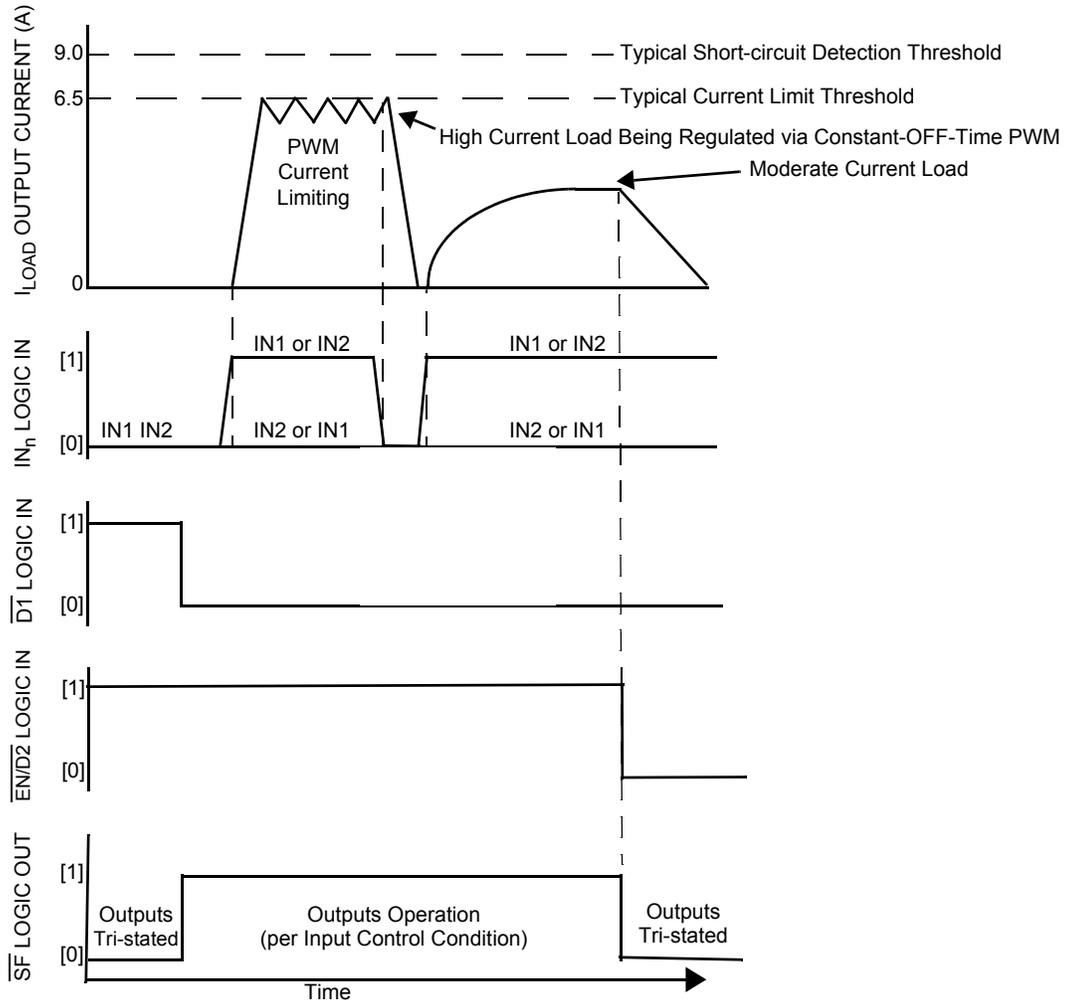


Figure 11. Operating States

**LOGIC COMMANDS AND REGISTERS**

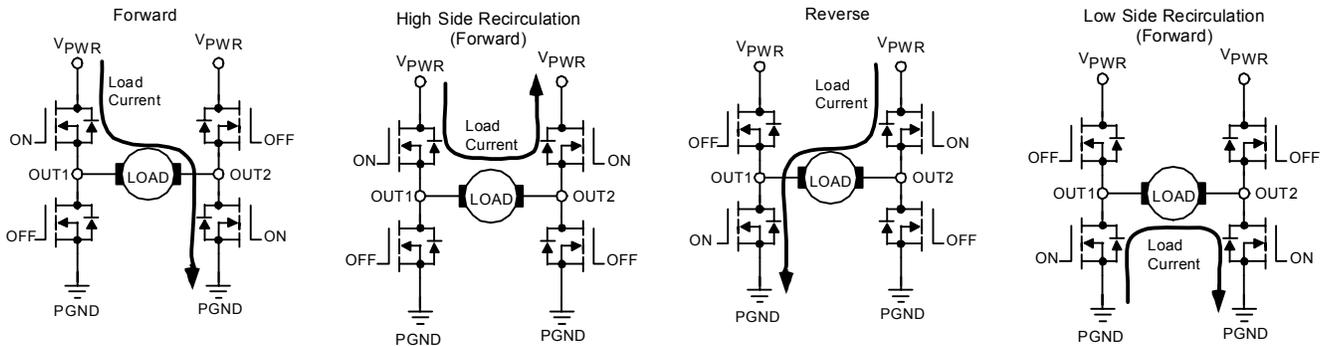
**Table 5. Truth Table**

The tri-state conditions and the status flag are reset using D1 or EN/D2. The truth table uses the following notations: L = LOW, H = HIGH, X = HIGH or LOW, and Z = High-impedance. All output power transistors are switched off.

Device State	Input Conditions				Status $\overline{SF}$	Outputs	
	EN/D2	D1	IN1	IN2		OUT1	OUT2
Forward	H	L	H	L	H	H	L
Reverse	H	L	L	H	H	L	H
Free Wheeling Low	H	L	L	L	H	L	L
Free Wheeling High	H	L	H	H	H	H	H
Disable 1 (D1)	H	H	X	X	L	Z	Z
IN1 Disconnected	H	L	Z	X	H	H	X
IN2 Disconnected	H	L	X	Z	H	X	H
D1 Disconnected	H	Z	X	X	L	Z	Z
Under-voltage Lockout <sup>(29)</sup>	H	X	X	X	L	Z	Z
Over-temperature <sup>(30)</sup>	H	X	X	X	L	Z	Z
Short-circuit <sup>(30)</sup>	H	X	X	X	L	Z	Z
Sleep Mode EN/D2	L	X	X	X	H	Z	Z
EN/D2 Disconnected	Z	X	X	X	H	Z	Z

Notes

- 29. In the event of an under-voltage condition, the outputs tri-state and status flag is SET logic LOW. Upon under-voltage recovery, status flag is reset automatically or automatically cleared and the outputs are restored to their original operating condition.
- 30. When a short-circuit or over-temperature condition is detected, the power outputs are tri-state latched-OFF independent of the input signals and the status flag is latched to logic LOW. To reset from this condition requires the toggling of either D1, EN/D2, or V<sub>PWR</sub>.



**Figure 12. 33931 Power Stage Operation**

## PROTECTION AND DIAGNOSTIC FEATURES

### SHORT-CIRCUIT PROTECTION

If an output short-circuit condition is detected, the power outputs tri-state (latch-OFF) independent of the input (IN1 and IN2) states, and the fault status output flag (SF) is SET to logic LOW. If the D1 input changes from logic HIGH to logic LOW, or if the EN/D2 input changes from logic LOW to logic HIGH, the output bridge will become operational again and the fault status flag will be reset (cleared) to a logic HIGH state.

The output stage will always switch into the mode defined by the input pins (IN1, IN2, D1, and EN/D2), provided the device junction temperature is within the specified operating temperature range.

### INTERNAL PWM CURRENT LIMITING

The maximum current flow under normal operating conditions should be less than 5.0 A. The instantaneous load currents will be limited to  $I_{LIM}$  via the internal PWM current limiting circuitry. When the  $I_{LIM}$  threshold current value is reached, the output stages are tri-stated for a fixed time ( $T_A$ ) of 20  $\mu$ s typical. Depending on the time constant associated with the load characteristics, the output current decreases during the tri-state duration until the next output ON cycle occurs.

The PWM current limit threshold value is dependent on the device junction temperature. When  $-40^{\circ}\text{C} < T_J < 160^{\circ}\text{C}$ ,  $I_{LIM}$  is between the specified minimum/maximum values. When  $T_J$  exceeds  $160^{\circ}\text{C}$ , the  $I_{LIM}$  threshold decreases to 4.2 A. Shortly above  $175^{\circ}\text{C}$  the device over-temperature circuit will detect  $T_{LIM}$  and an over-temperature shutdown will occur. This feature implements a graceful degradation of operation before thermal shutdown occurs, thus allowing for intermittent unexpected mechanical loads on the motor's gear-reduction train to be handled.

**Important** Die temperature excursions above  $150^{\circ}\text{C}$  are permitted only for non-repetitive durations  $< 30$  seconds. Provision must be made at the system level to prevent prolonged operation in the current-foldback region.

### OVER-TEMPERATURE SHUTDOWN AND HYSTERESIS

If an over-temperature condition occurs, the power outputs are tri-stated (latched-OFF) and the fault status flag (SF) is SET to logic LOW.

To reset from this condition, D1 must change from logic HIGH to logic LOW, or EN/D2 must change from logic LOW to logic HIGH. When reset, the output stage switches ON again, provided that the junction temperature is now below the over-temperature threshold limit minus the hysteresis.

**Important** Resetting from the fault condition will clear the fault status flag. Powering down and powering up the device will also reset the 33931 from the fault condition.

### OUTPUT AVALANCHE PROTECTION

If VPWR were to become an open circuit, the outputs would likely tri-state simultaneously due to the disable logic. This could result in an unclamped inductive discharge. The VPWR input to the 33931 should not exceed 40 V during this transient condition, to prevent electrical overstress of the output drivers. This can be accomplished with a zener clamp or MOV, and/or an appropriately valued input capacitor with sufficiently low ESR (see [Figure 13](#)).

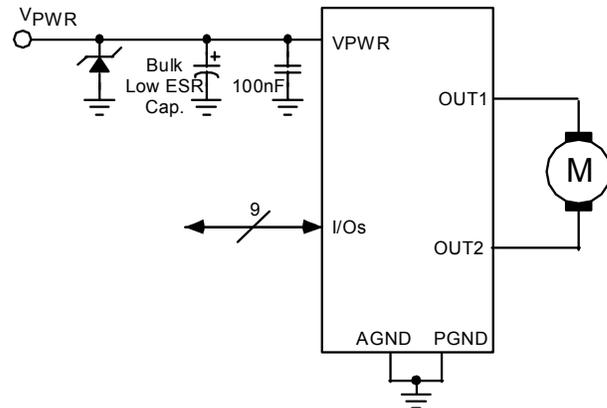


Figure 13. Avalanche Protection

## TYPICAL APPLICATIONS

### INTRODUCTION

A typical application schematic is shown in [Figure 14](#). For precision high-current applications in harsh, noisy

environments, the  $V_{PWR}$  by-pass capacitor may need to be substantially larger.

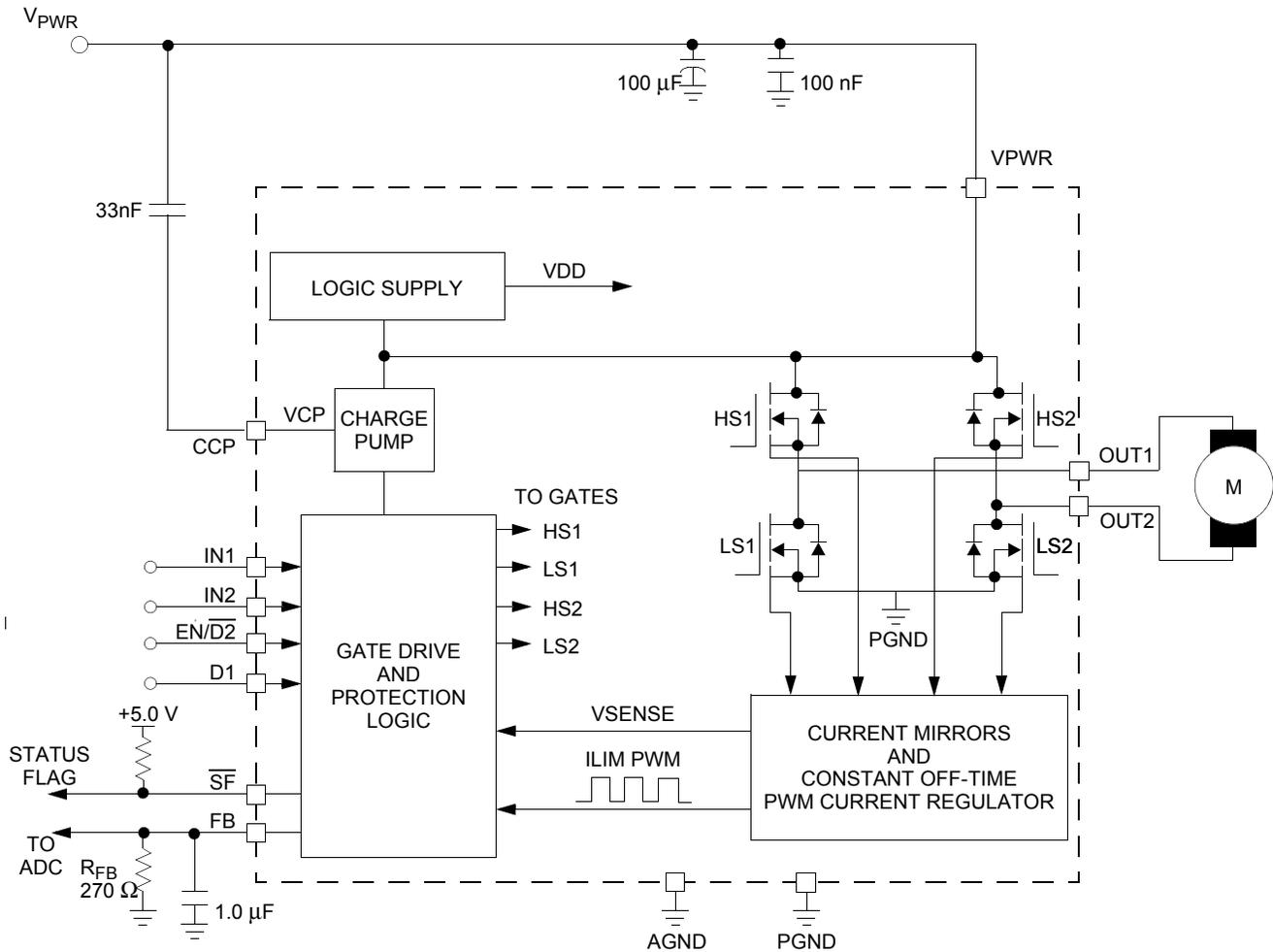
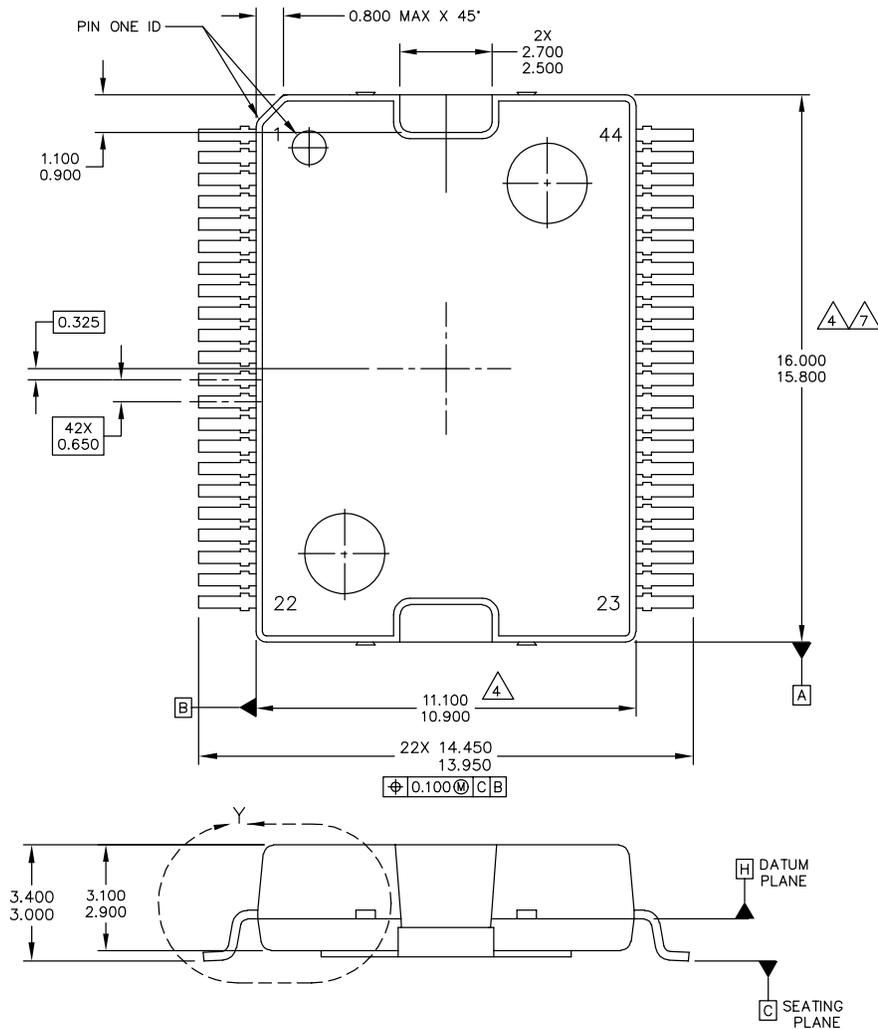


Figure 14. 33931 Typical Application Schematic

# PACKAGING

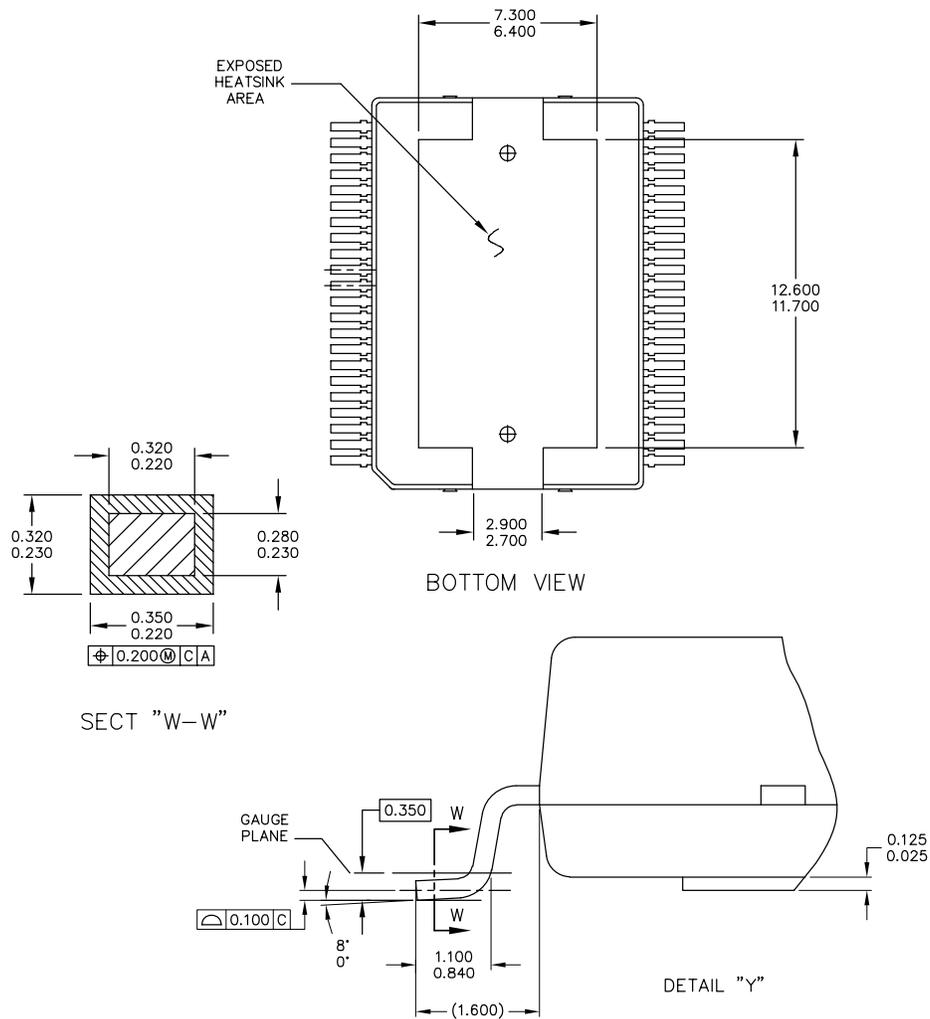
## PACKAGE DIMENSIONS

For the most current package revision, visit [www.freescale.com](http://www.freescale.com) and perform a keyword search using the 98Axxxxxxx listed below.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
TITLE: 44 LEAD HSOP W/PROTRUDING HEATSINK	DOCUMENT NO: 98ARH98330A	REV: B	
	CASE NUMBER: 1291-02	16 MAR 2005	
	STANDARD: NON-JEDEC		

**VW SUFFIX**  
44-PIN  
98ARH98330A  
REVISION B



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
TITLE: 44 LEAD HSOP W/PROTRUDING HEATSINK	DOCUMENT NO: 98ARH98330A	REV: B	
	CASE NUMBER: 1291-02	16 MAR 2005	
	STANDARD: NON-JEDEC		

**VW SUFFIX**  
44-PIN  
98ARH98330A  
REVISION B

**REVISION HISTORY**

REVISION	DATE	DESCRIPTION
1.0	2/2008	<ul style="list-style-type: none"><li>Initial Release</li></ul>
2.0	12/2008	<ul style="list-style-type: none"><li>Updated Freescale for and style</li><li>Removed PC33931VW/R2 from the ordering information and added MC33931VW/R2</li><li>Changes Max <math>R_{DS(ON)}</math> from 225 to 235 mOhm in the document</li><li>Changed <a href="#">Peak Package Reflow Temperature During Reflow</a><sup>(7), (8)</sup></li><li>Changed <a href="#">Approximate Junction-to-Case Thermal Resistance</a><sup>(9)</sup></li><li>In <a href="#">SHORT-CIRCUIT PROTECTION</a>, changed <math>\overline{D2}</math> to EN<math>\overline{D2}</math></li></ul>

## **How to Reach Us:**

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **Web Support:**

<http://www.freescale.com/support>

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor, Inc.  
Technical Information Center, EL516  
2100 East Elliot Road  
Tempe, Arizona 85284  
+1-800-521-6274 or +1-480-768-2130  
[www.freescale.com/support](http://www.freescale.com/support)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[www.freescale.com/support](http://www.freescale.com/support)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor China Ltd.  
Exchange Building 23F  
No. 118 Jianguo Road  
Chaoyang District  
Beijing 100022  
China  
+86 10 5879 8000  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-441-2447 or 303-675-2140  
Fax: 303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2008. All rights reserved.