



K10 Sub-Family Data Sheet

Supports the following:

MK10DX128ZVLQ10,
MK10DX128ZVMD10,
MK10DX256ZVLQ10,
MK10DX256ZVMD10,
MK10DN512ZVLQ10,
MK10DN512ZVMD10

Features

- Operating Characteristics
 - Voltage range: 1.71 to 3.6 V
 - Flash write voltage range: 1.71 to 3.6 V
 - Temperature range (ambient): -40 to 105°C
- Performance
 - Up to 100 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz
- Memories and memory interfaces
 - Up to 512 KB program flash memory on non-FlexMemory devices
 - Up to 128 KB RAM
 - Serial programming interface (EzPort)
 - FlexBus external bus interface
- Clocks
 - 3 to 32 MHz crystal oscillator
 - 32 kHz crystal oscillator
 - Multi-purpose clock generator
- System peripherals
 - 10 low-power modes to provide power optimization based on application requirements
 - Memory protection unit with multi-master protection
 - 16-channel DMA controller, supporting up to 64 request sources
 - External watchdog monitor
 - Software watchdog
 - Low-leakage wakeup unit
- Security and integrity modules
 - Hardware CRC module to support fast cyclic redundancy checks
 - 128-bit unique identification (ID) number per chip
- Human-machine interface
 - Low-power hardware touch sensor interface (TSI)
 - General-purpose input/output
- Analog modules
 - Two 16-bit SAR ADCs
 - Programmable gain amplifier (PGA) (up to x64) integrated into each ADC
 - Two 12-bit DACs
 - Three analog comparators (CMP) containing a 6-bit DAC and programmable reference input
 - Voltage reference
- Timers
 - Programmable delay block
 - Eight-channel motor control/general purpose/PWM timer
 - Two 2-channel quadrature decoder/general purpose timers
 - Periodic interrupt timers
 - 16-bit low-power timer
 - Carrier modulator transmitter
 - Real-time clock
- Communication interfaces
 - Two Controller Area Network (CAN) modules
 - Three SPI modules
 - Two I2C modules
 - Six UART modules
 - Secure Digital host controller (SDHC)
 - I2S module

K10P144M100SF2



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Preliminary



Table of Contents

1 Ordering parts.....	3	5.3.2 Thermal attributes.....	20
1.1 Determining valid orderable parts.....	3	6 Peripheral operating requirements and behaviors.....	21
2 Part identification.....	3	6.1 Core modules.....	22
2.1 Description.....	3	6.1.1 Debug trace timing specifications.....	22
2.2 Format.....	3	6.1.2 JTAG electricals.....	23
2.3 Fields.....	3	6.2 System modules.....	26
2.4 Example.....	4	6.3 Clock modules.....	26
3 Terminology and guidelines.....	4	6.3.1 MCG specifications.....	26
3.1 Definition: Operating requirement.....	4	6.3.2 Oscillator electrical specifications.....	28
3.2 Definition: Operating behavior.....	5	6.3.3 32kHz Oscillator Electrical Characteristics.....	31
3.3 Definition: Attribute.....	5	6.4 Memories and memory interfaces.....	31
3.4 Definition: Rating.....	6	6.4.1 Flash (FTFL) electrical specifications.....	31
3.5 Result of exceeding a rating.....	6	6.4.2 EzPort Switching Specifications.....	33
3.6 Relationship between ratings and operating requirements.....	6	6.4.3 Flexbus Switching Specifications.....	34
3.7 Guidelines for ratings and operating requirements.....	7	6.5 Security and integrity modules.....	37
3.8 Definition: Typical value.....	7	6.6 Analog.....	37
3.9 Typical value conditions.....	8	6.6.1 ADC electrical specifications.....	37
4 Ratings.....	8	6.6.2 CMP and 6-bit DAC electrical specifications.....	45
4.1 Thermal handling ratings.....	9	6.6.3 12-bit DAC electrical characteristics.....	47
4.2 Moisture handling ratings.....	9	6.6.4 Voltage reference electrical specifications.....	50
4.3 ESD handling ratings.....	9	6.7 Timers.....	51
4.4 Voltage and current operating ratings.....	9	6.8 Communication interfaces.....	52
5 General.....	10	6.8.1 CAN switching specifications.....	52
5.1 Nonswitching electrical specifications.....	10	6.8.2 DSPI switching specifications (low-speed mode).....	52
5.1.1 Voltage and current operating requirements.....	10	6.8.3 DSPI switching specifications (high-speed mode).....	53
5.1.2 LVD and POR operating requirements.....	11	6.8.4 I2C switching specifications.....	55
5.1.3 Voltage and current operating behaviors.....	12	6.8.5 UART switching specifications.....	55
5.1.4 Power mode transition operating behaviors.....	13	6.8.6 SDHC specifications.....	55
5.1.5 Power consumption operating behaviors.....	14	6.8.7 I2S switching specifications.....	56
5.1.6 EMC radiated emissions operating behaviors.....	17	6.9 Human-machine interfaces (HMI).....	58
5.1.7 Designing with radiated emissions in mind.....	18	6.9.1 TSI electrical specifications.....	58
5.1.8 Capacitance attributes.....	18	7 Dimensions.....	59
5.2 Switching specifications.....	18	7.1 Obtaining package dimensions.....	59
5.2.1 Device clock specifications.....	18	8 Pinout.....	60
5.2.2 General switching specifications.....	19	8.1 K10 Signal Multiplexing and Pin Assignments.....	60
5.3 Thermal specifications.....	20	8.2 K10 Pinouts.....	66
5.3.1 Thermal operating requirements.....	20	9 Revision History.....	68

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to <http://www.freescale.com> and perform a part number search for the following device numbers: PK10 and MK10.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	- M = Fully qualified, general market flow - P = Prequalification
K##	Kinetis family	K10
A	Key attribute	- D = Cortex-M4 w/ DSP - F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	- N = Program flash only - X = Program flash and FlexMemory

Table continues on the next page...

Terminology and guidelines

Field	Description	Values
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB • 256 = 256 KB • 512 = 512 KB • 1M0 = 1 MB
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = -40 to 105 • C = -40 to 85
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LF = 48 LQFP (7 mm x 7 mm) • EX = 64 QFN (9 mm x 9 mm) • LH = 64 LQFP (10 mm x 10 mm) • LK = 80 LQFP (12 mm x 12 mm) • MB = 81 MAPBGA (8 mm x 8 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm) • MF = 196 MAPBGA (15 mm x 15 mm) • MJ = 256 MAPBGA (17 mm x 17 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MK10DN512ZVMD10

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

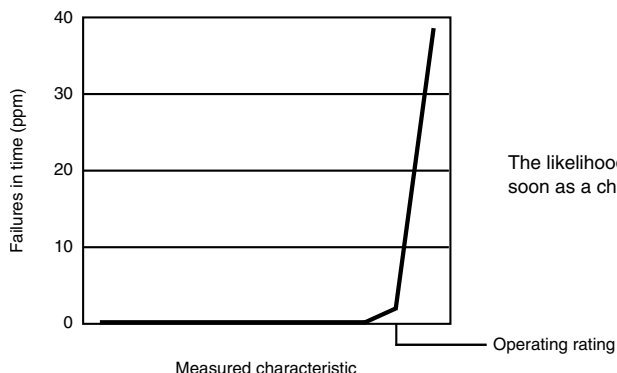
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	−0.3	1.2	V

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

3.6 Relationship between ratings and operating requirements

Operating or handling rating (min.)		Operating requirement (min.)		Operating requirement (max.)		Operating or handling rating (max.)	
Fatal range - Probable permanent failure	Limited operating range - No permanent failure - Possible decreased life - Possible incorrect operation	Normal operating range - No permanent failure - Correct operation	Limited operating range - No permanent failure - Possible decreased life - Possible incorrect operation	Fatal range - Probable permanent failure			
	Handling range - No permanent failure						

3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

3.8.1 Example 1

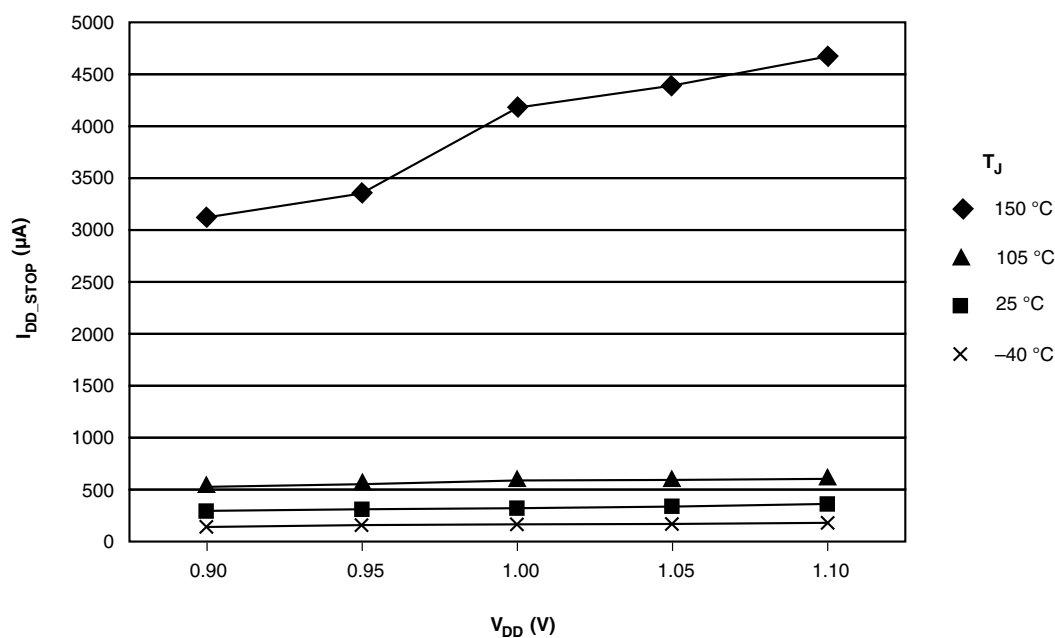
This is an example of an operating behavior that includes a typical value:

Ratings

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	$^{\circ}C$
V_{DD}	3.3 V supply voltage	3.3	V

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	–55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	–100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	–0.3	3.8	V
I _{DD}	Digital supply current	—	185	mA
V _{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	–0.3	5.5	V

Table continues on the next page...

General

Symbol	Description	Min.	Max.	Unit
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 Nonswitching electrical specifications

5.1.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	$0.7 \times V_{DD}$	—	V	
		$0.75 \times V_{DD}$	—	V	
V_{IL}	Input low voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	—	$0.35 \times V_{DD}$	V	
		—	$0.3 \times V_{DD}$	V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{ICDIO}	Digital pin negative DC injection current — single pin $V_{IN} < V_{SS}-0.3\text{V}$	-5	—	mA	1
I_{ICAIO}	Analog ² , EXTAL, and XTAL pin DC injection current — single pin $V_{IN} < V_{SS}-0.3\text{V}$ (Negative current injection) $V_{IN} > V_{DD}+0.3\text{V}$ (Positive current injection)	-5	—	mA	3
		—	+5		

Table continues on the next page...

Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{Ccont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins - Negative current injection - Positive current injection	-25 —	— +25	mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	TBD	—	V	

- All 5 volt tolerant digital I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{DIO_MIN} ($=V_{SS}-0.3V$) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO_MIN}-V_{IN})/|I_{IC}|$.
- Analog pins are defined as pins that do not have an associated general purpose I/O port function.
- All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is greater than V_{AIO_MIN} ($=V_{SS}-0.3V$) and V_{IN} is less than V_{AIO_MAX} ($=V_{DD}+0.3V$) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{IC}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO_MAX})/|I_{IC}|$. Select the larger of these two calculated resistances.

5.1.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	TBD	1.1	TBD	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	TBD	2.56	TBD	V	
V_{LVW1H}	Low-voltage warning thresholds — high range Level 1 falling (LVWV=00)	TBD	2.70	TBD	V	1
V_{LVW2H}	Level 2 falling (LVWV=01)	TBD	2.80	TBD	V	
V_{LVW3H}	Level 3 falling (LVWV=10)	TBD	2.90	TBD	V	
V_{LVW4H}	Level 4 falling (LVWV=11)	TBD	3.00	TBD	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range		60		mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	TBD	1.60	TBD	V	
V_{LVW1L}	Low-voltage warning thresholds — low range Level 1 falling (LVWV=00)	TBD	1.80	TBD	V	1
V_{LVW2L}	Level 2 falling (LVWV=01)	TBD	1.90	TBD	V	
V_{LVW3L}	Level 3 falling (LVWV=10)	TBD	2.00	TBD	V	
V_{LVW4L}	Level 4 falling (LVWV=11)	TBD	2.10	TBD	V	

Table continues on the next page...

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range		40		mV	
V _{BG}	Bandgap voltage reference	TBD	1.00	TBD	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	TBD	1000	TBD	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR_VBAT}	Falling VBAT supply POR detect voltage	TBD	1.1	TBD	V	

5.1.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{OH}	Output high voltage — high drive strength				
	• 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = -10mA	V _{DD} - 0.5	—	V	
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = -3mA	V _{DD} - 0.5	—	V	
	Output high voltage — low drive strength				
V _{OL}	• 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = -2mA	V _{DD} - 0.5	—	V	
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = -0.6mA	V _{DD} - 0.5	—	V	
	Output low voltage — high drive strength				
	• 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 10mA	—	0.5	V	
I _{OLT}	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 3mA	—	0.5	V	
	Output low voltage — low drive strength				
	• 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 2mA	—	0.5	V	
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 0.6mA	—	0.5	V	
I _{OLT}	Output low current total for all ports	—	100	mA	
I _{IN}	Input leakage current (per pin) for full temperature range	—	1	μA	1
I _{IN}	Input leakage current (per pin) at 25°C	—	TBD	μA	1
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
R _{PU}	Internal pullup resistors	20	50	kΩ	2

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
R _{PD}	Internal pulldown resistors	20	50	kΩ	3

1. Measured at V_{DD}=3.6V
2. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{SS}
3. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{DD}

5.1.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V _{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	1
	RUN → VLLS1 → RUN				
	• RUN → VLLS1	—	4.1	μs	
	• VLLS1 → RUN	—	123.8	μs	
	RUN → VLLS2 → RUN				
	• RUN → VLLS2	—	4.1	μs	
	• VLLS2 → RUN	—	49.3	μs	
	RUN → VLLS3 → RUN				
	• RUN → VLLS3	—	4.1	μs	
	• VLLS3 → RUN	—	49.2	μs	
	RUN → LLS → RUN				
	• RUN → LLS	—	4.1	μs	
	• LLS → RUN	—	5.9	μs	
	RUN → STOP → RUN				
	• RUN → STOP	—	4.1	μs	
	• STOP → RUN	—	4.2	μs	

Table continues on the next page...

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	RUN → VLPS → RUN				
	• RUN → VLPS	—	4.1	μs	
	• VLPS → RUN	—	5.8	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.1.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	TBD	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash	—	40	TBD	mA	2
	• @ 1.8V	—	42	TBD	mA	
	• @ 3.0V					
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash	—	55	TBD	mA	3
	• @ 1.8V	—	56	TBD	mA	
	• @ 3.0V					
I _{DD_RUN_M AX}	Run mode current — all peripheral clocks enabled and peripherals active, code executing from flash	—	66	TBD	mA	4
	• @ 1.8V	—	66	TBD	mA	
	• @ 3.0V	—	TBD	TBD	mA	
	• @ 25°C					
	• @ 125°C					
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	35	TBD	mA	2
I _{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	15	TBD	mA	5
I _{DD_STOP}	Stop mode current at 3.0 V	—	0.4	TBD	mA	
	• @ -40 to 25°C	—	TBD	TBD	mA	
	• @ 70°C	—	TBD	TBD	mA	
	• @ 105°C	—	TBD	TBD	mA	
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.25	TBD	mA	6

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	TBD	TBD	mA	7
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V	—	1.05	TBD	mA	8
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	—	50	TBD	μA	
		—	TBD	TBD	μA	
		—	TBD	TBD	μA	
		—	TBD	TBD	μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	—	12	TBD	μA	9
		—	TBD	TBD	μA	
		—	TBD	TBD	μA	
		—	TBD	TBD	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	—	8	TBD	μA	9
		—	TBD	TBD	μA	
		—	TBD	TBD	μA	
		—	TBD	TBD	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	—	4	TBD	μA	
		—	TBD	TBD	μA	
		—	TBD	TBD	μA	
		—	TBD	TBD	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	—	2	TBD	μA	
		—	TBD	TBD	μA	
		—	TBD	TBD	μA	
		—	TBD	TBD	μA	
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	—	0.7	TBD	μA	10
		—	TBD	TBD	μA	
		—	TBD	TBD	μA	
		—	TBD	TBD	μA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, but peripherals are not in active operation.
4. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz FlexBus and flash clock. MCG configured for FEI mode.
6. 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.

General

- 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
- 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- Data reflects devices with 128 KB of RAM. For devices with 64 KB of RAM, power consumption is reduced by 2 μ A. For devices with 32 KB of RAM, power consumption is reduced by 3 μ A.
- Includes 32kHz oscillator current and RTC operation.

5.1.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FEI mode (39.0625 kHz IRC), except for 1 MHz core (FBE)
- All peripheral clocks disabled except FTFL
- LVD disabled
- No GPIOs toggled
- Code execution from flash

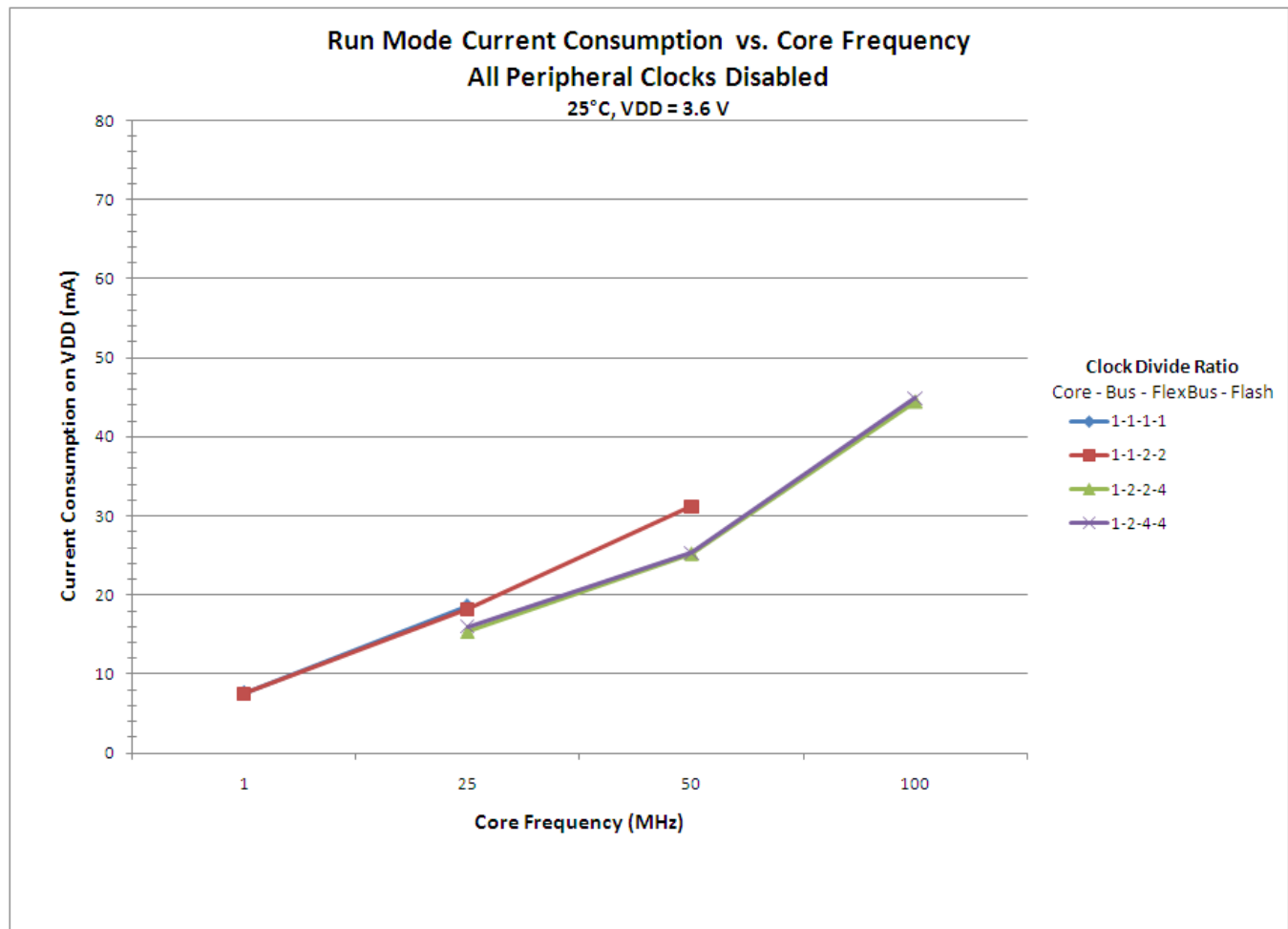


Figure 1. Run mode supply current vs. core frequency — all peripheral clocks disabled

The following data was measured under these conditions:

- MCG in FEI mode (39.0625 kHz IRC), except for 1 MHz core (FBE)
- All peripheral clocks enabled but peripherals are not in active operation
- LVD disabled
- No GPIOs toggled
- Code execution from flash

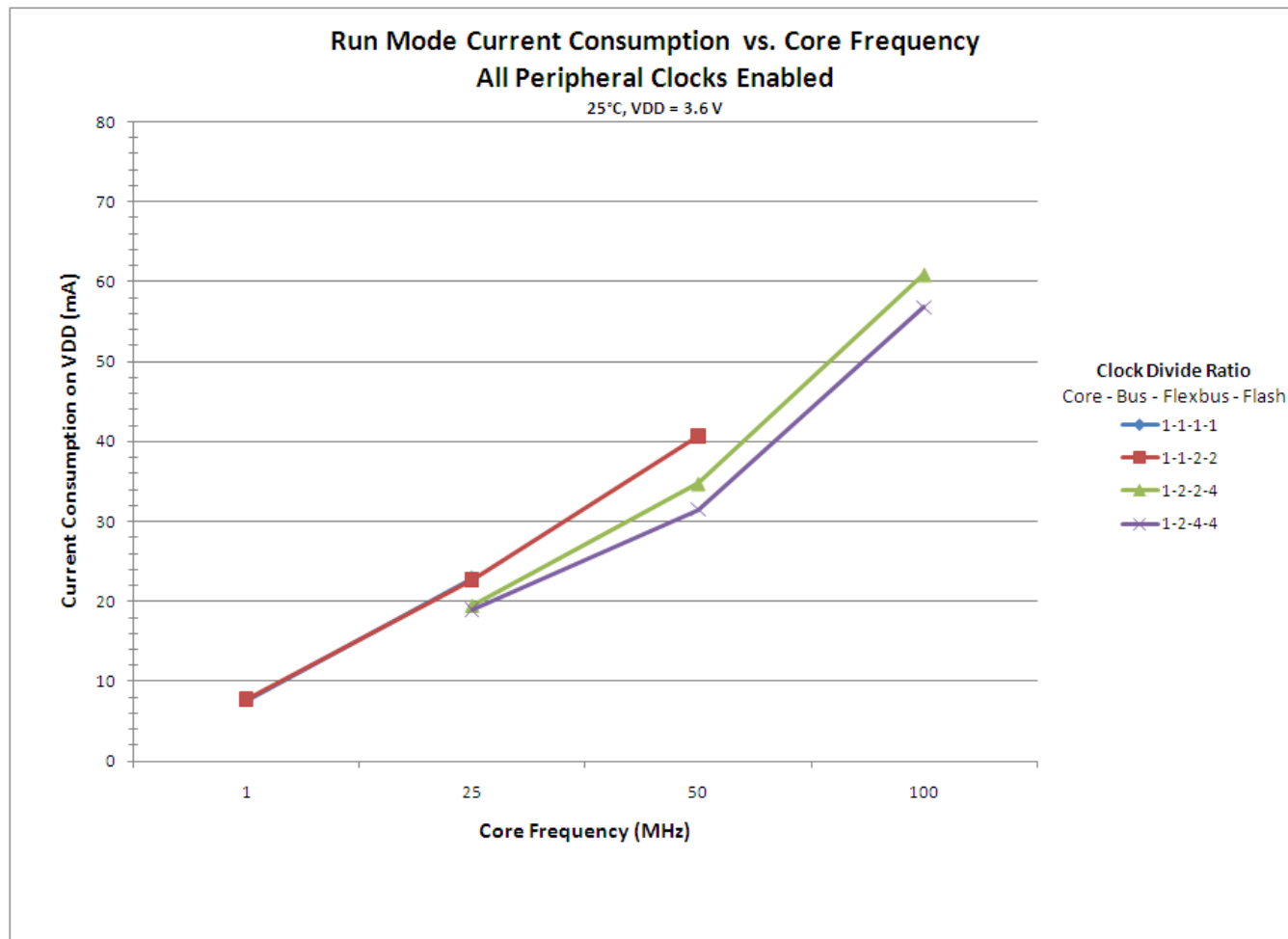


Figure 2. Run mode supply current vs. core frequency — all peripheral clocks enabled

5.1.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	TBD	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	TBD	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	TBD	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	TBD	dBμV	
V _{RE_IEC_SAE}	IEC and SAE level	0.15–1000	TBD	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions*, IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*, and SAE Standard J1752-3, *Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method*.
2. V_{DD} = 3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = 96 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*, and Appendix D of SAE Standard J1752-3, *Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method*.

5.1.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to <http://www.freescale.com>.
2. Perform a keyword search for “EMC design.”

5.1.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN_A}	Input capacitance: analog pins	—	7	pF
C _{IN_D}	Input capacitance: digital pins	—	7	pF

5.2 Switching specifications

5.2.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f _{SYS}	System and core clock	—	100	MHz	
f _{BUS}	Bus clock	—	50	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
f _{FLASH}	Flash clock	—	25	MHz	
f _{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode					
f _{SYS}	System and core clock	—	2	MHz	
f _{BUS}	Bus clock	—	2	MHz	
FB_CLK	FlexBus clock	—	2	MHz	
f _{FLASH}	Flash clock	—	1	MHz	
f _{LPTMR}	LPTMR clock	—	25	MHz	

5.2.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, and I²C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	16	—	ns	2
	External reset pulse width (digital glitch filter disabled)	100	—	ns	2
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	

Table continues on the next page...

Table 10. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	Port rise and fall time (high drive strength) - Slew disabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$ - Slew enabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$	—	12	ns	3
		—	TBD	ns	
		—	36	ns	
		—	TBD	ns	
	Port rise and fall time (low drive strength) - Slew disabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$ - Slew enabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$	—	32	ns	4
		—	TBD	ns	
		—	36	ns	
		—	TBD	ns	

1. The greater synchronous and asynchronous timing must be met.

2. This is the shortest pulse that is guaranteed to be recognized.

3. 75pF load

4. 15pF load

5.3 Thermal specifications

5.3.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	125	°C
T_A	Ambient temperature	−40	105	°C

5.3.2 Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	52	50	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	44	30	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	43	41	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	38	27	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	33	17	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	11	10	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

All digital I/O switching characteristics assume:

1. output pins
 - have $C_L=30\text{pF}$ loads,
 - are configured for fast slew rate ($\text{PORTx_PCRn[SRE]}=0$), and
 - are configured for high drive strength ($\text{PORTx_PCRn[DSE]}=1$)
2. input pins
 - have their passive filter disabled ($\text{PORTx_PCRn[PFE]}=0$)

6.1 Core modules

6.1.1 Debug trace timing specifications

Table 12. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	—	ns
T_h	Data hold	2	—	ns

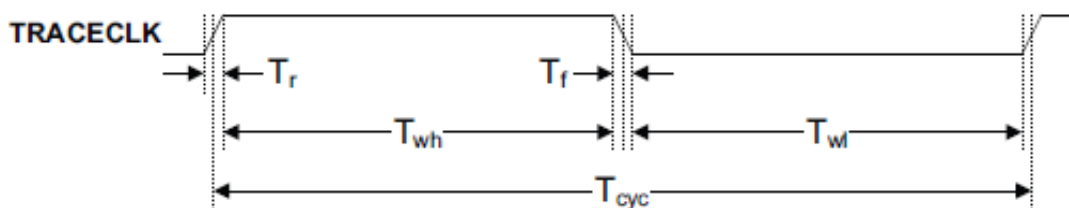


Figure 3. TRACE_CLKOUT specifications

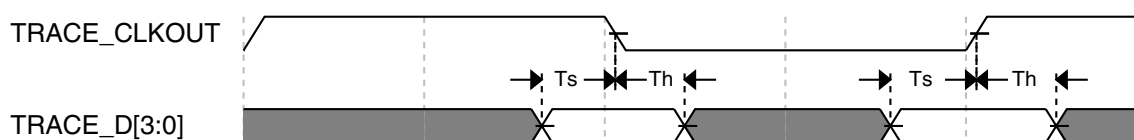


Figure 4. Trace data specifications

6.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	0 0 0	10 25 50	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	50 20 10	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

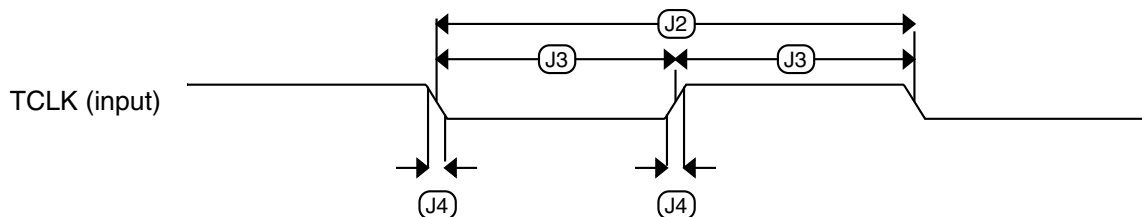
Table 14. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	0 0 0	10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns

Table continues on the next page...

Table 14. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

**Figure 5. Test clock input timing**

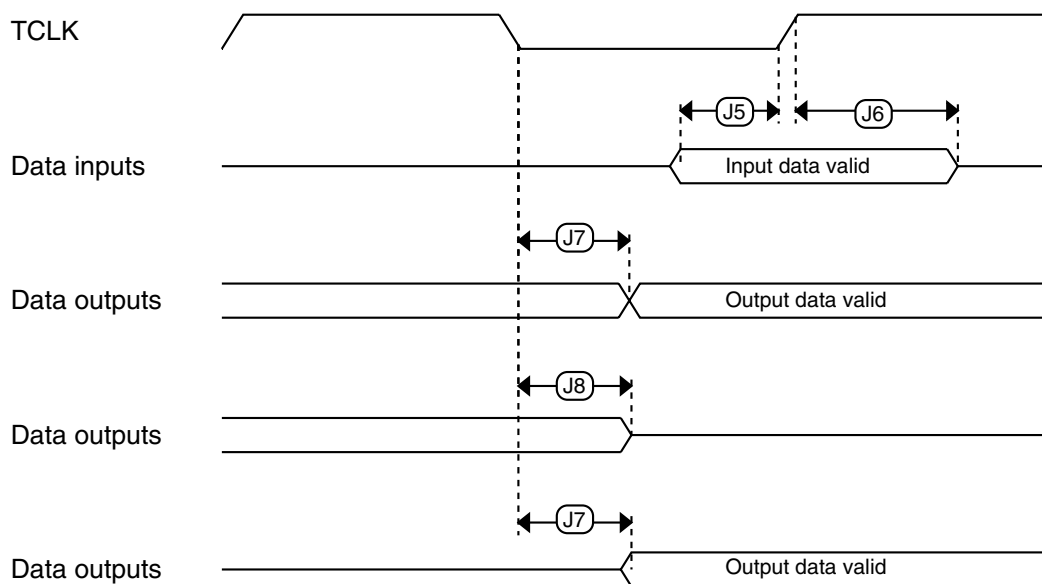


Figure 6. Boundary scan (JTAG) timing

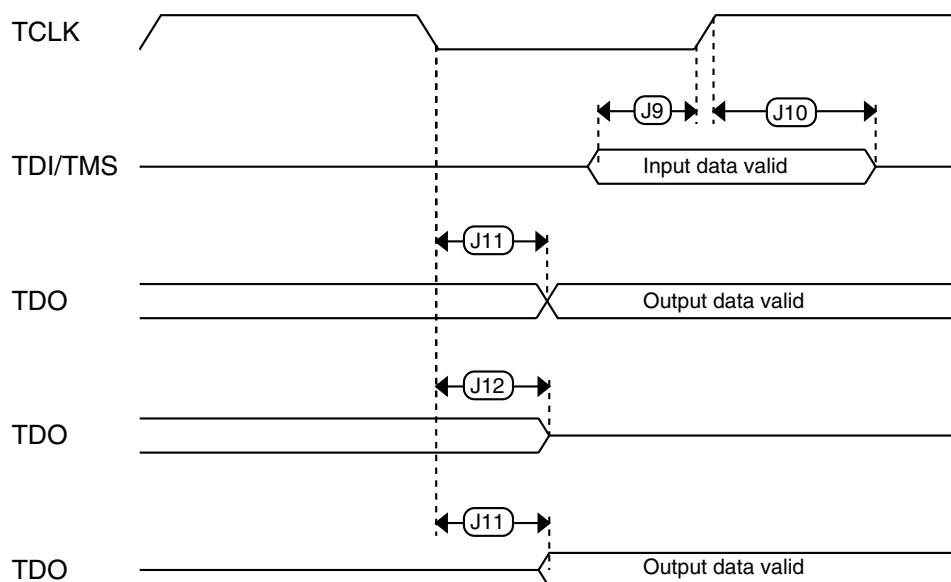


Figure 7. Test Access Port timing

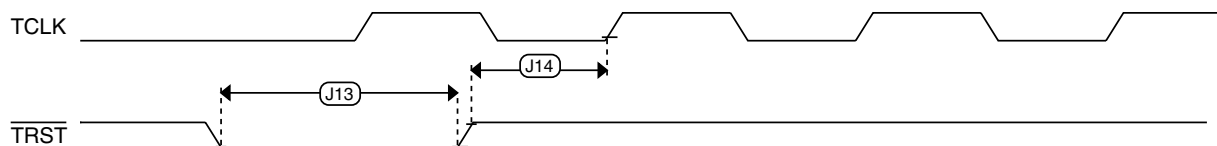


Figure 8. TRST timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{ints_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25°C	—	32.768	—	kHz	
$f_{\text{ints_t}}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
I_{ints}	Internal reference (slow clock) current	—	TBD	—	μA	
t_{refsts}	Internal reference (slow clock) startup time	—	TBD	4	μs	1
$\Delta f_{\text{dco_res_t}}$	Resolution of trimmed DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.1	± 0.3	% f_{dco}	2
$\Delta f_{\text{dco_res_t}}$	Resolution of trimmed DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	% f_{dco}	2
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+ 0.5 - 1.0	± 3.5	% f_{dco}	2
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.5	± TBD	% f_{dco}	2
$f_{\text{intf_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	3.4	—	4	MHz	
$f_{\text{intf_t}}$	Internal reference frequency (fast clock) — user trimmed	3	—	5	MHz	

Table continues on the next page...

Table 15. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
I _{intf}	Internal reference (fast clock) current		—	TBD	—	μA	
t _{irefstf}	Internal reference startup time (fast clock)		—	TBD	TBD	μs	1
f _{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f _{ints_t}	—	—	kHz	
f _{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f _{ints_t}	—	—	kHz	
FLL							
f _{fill_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fill_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) 1280 × f _{fill_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fill_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fill_ref}	80	83.89	100	MHz	
f _{dco_t_DMx3} 2	DCO output frequency	Low range (DRS=00) 732 × f _{fill_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) 1464 × f _{fill_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f _{fill_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f _{fill_ref}	—	95.98	—	MHz	
J _{cyc_fill}	FLL period jitter		—	TBD	TBD	ps	7
J _{acc_fill}	FLL accumulated jitter of DCO output over a 1μs time window		—	TBD	TBD	ps	7
t _{fill_acquire}	FLL target frequency acquisition time		—	—	1	ms	8
PLL							
f _{vco}	VCO operating frequency		48.0	—	100	MHz	
I _{pll}	PLL operating current PLL @ 96 MHz (f_{osc_hi_1} = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	μA	9
I _{pll}	PLL operating current PLL @ 48 MHz (f_{osc_hi_1} = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	μA	9
f _{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	

Table continues on the next page...

Table 15. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{cyc_pll}	PLL period jitter (RMS) $f_{vco} = 48 \text{ MHz}$ $f_{vco} = 100 \text{ MHz}$	—	120	—	ps	10
		—	50	—	ps	
J_{acc_pll}	PLL accumulated jitter over 1 μ s (RMS) $f_{vco} = 48 \text{ MHz}$ $f_{vco} = 100 \text{ MHz}$	—	1350	—	ps	10
		—	600	—	ps	
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$0.15 + \frac{1075}{f_{pll_ref}}$	ms	11

1. The startup time is defined as the time between the IRC being enabled, either by the MCG or by the IRCLKEN bit being set, and the first edge of the internal reference clock.
2. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification was obtained at TBD frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
9. Excludes any oscillator currents that are also consuming power while PLL is in operation.
10. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
11. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

6.3.2.1 Oscillator DC electrical specifications

Table 16. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	

Table continues on the next page...

Table 16. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (only RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I _{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
	• 4 MHz	—	400	—	μA	
	• 8 MHz (only RANGE=01)	—	500	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C _x	EXTAL load capacitance	—	—	—		2, 3
C _y	XTAL load capacitance	—	—	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	

Table continues on the next page...

Table 16. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD} =3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x, C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.2.2 Oscillator frequency specifications

Table 17. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	2, 3
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL
2. Proper PC board layout procedures must be followed to achieve specifications.

- Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

6.3.3 32kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

6.3.3.1 32kHz oscillator DC electrical specifications

Table 18. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	2.5	—	pF
C_{load}	Internal load capacitance (programmable)	—	15	—	pF
V_{pp} ¹	Peak-to-peak amplitude of oscillation	—	0.6	—	V

- The EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32kHz oscillator frequency specifications

Table 19. 32kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1

- Proper PC board layout procedures must be followed to achieve specifications.

6.4 Memories and memory interfaces

6.4.1 Flash (FTFL) electrical specifications

This section describes the electrical characteristics of the FTFL module.

6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 20. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{pgm}4}$	Longword Program high-voltage time	—	20	TBD	μs	
$t_{h\text{versscr}}$	Sector Erase high-voltage time	—	20	100	ms	1
$t_{h\text{versblk}256\text{k}}$	Erase Block high-voltage time for 256 KB	—	160	800	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands

Table 21. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{\text{rd}1\text{blk}256\text{k}}$	Read 1s Block execution time • 256 KB data flash	—	—	1.4	ms	
$t_{\text{rd}1\text{sec}2\text{k}}$	Read 1s Section execution time (flash sector)	—	—	40	μs	1
t_{pgmchk}	Program Check execution time	—	—	35	μs	1
$t_{\text{rd}r\text{src}}$	Read Resource execution time	—	—	35	μs	1
$t_{\text{pgm}4}$	Program Longword execution time	—	50	TBD	μs	
$t_{\text{ersblk}256\text{k}}$	Erase Flash Block execution time • 256 KB data flash	—	160	800	ms	2
t_{ersscr}	Erase Flash Sector execution time	—	20	100	ms	2
$t_{\text{pgmsec}512}$	Program Section execution time • 512 B flash • 1 KB flash • 2 KB flash	—	TBD	TBD	ms	
$t_{\text{pgmsec}1\text{k}}$		—	TBD	TBD	ms	
$t_{\text{pgmsec}2\text{k}}$		—	TBD	TBD	ms	
$t_{\text{rd}1\text{all}}$	Read 1s All Blocks execution time	—	—	2.8	ms	
$t_{\text{rd}o\text{nce}}$	Read Once execution time	—	—	35	μs	1
$t_{\text{pgm}o\text{nce}}$	Program Once execution time	—	50	TBD	μs	
t_{ersall}	Erase All Blocks execution time	—	320	1600	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	μs	1
$t_{\text{swap}x01}$	Swap Control execution time • control code 0x01 • control code 0x02 • control code 0x04 • control code 0x08	—	TBD	TBD	μs	
$t_{\text{swap}x02}$		—	TBD	TBD	μs	
$t_{\text{swap}x04}$		—	TBD	TBD	μs	
$t_{\text{swap}x08}$		—	TBD	TBD	μs	

1. Assumes 25MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

6.4.1.3 Flash (FTFL) current and power specifications

Table 22. Flash (FTFL) current and power specifications

Symbol	Description	Typ.	Unit
I _{DD_PGM}	Worst case programming current in program flash	10	mA

6.4.1.4 Reliability specifications

Table 23. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
t _{nvmretp10k}	Data retention after up to 10 K cycles	5	TBD	—	years	2
t _{nvmretp1k}	Data retention after up to 1 K cycles	10	TBD	—	years	2
t _{nvmretp100}	Data retention after up to 100 cycles	15	TBD	—	years	2
n _{nvmcycp}	Cycling endurance	10 K	TBD	—	cycles	3

1. Typical data retention values are based on intrinsic capability of the technology measured at high temperature derated to 25°C. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618.
2. Data retention is based on T_{avg} = 55°C (temperature profile over the lifetime of the application).
3. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.

6.4.2 EzPort Switching Specifications

Table 24. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	f _{sys} /2	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	f _{sys} /8	MHz
EP2	EZP_CS negation to next EZP_CS assertion	2 x t _{EZP_CK}	—	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid (setup)	—	12	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns

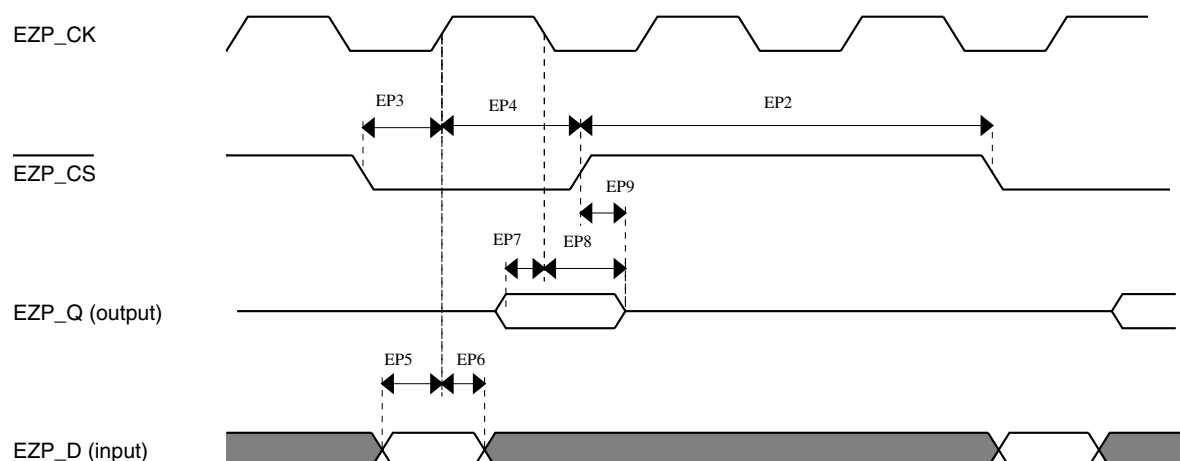


Figure 9. EzPort Timing Diagram

6.4.3 Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 25. Flexbus limited range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	50	MHz	
FB1	Clock period	20	—	ns	
FB2	Address, data, and control output valid	—	11.5	ns	1
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	8.5	—	ns	2
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}}_n$, $\overline{\text{FB_CS}}_n$, $\overline{\text{FB_OE}}$, FB_R/W, $\overline{\text{FB_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB_TS}}$.

2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

Table 26. Flexbus full range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	TBD	MHz	
FB1	Clock period	TBD	—	ns	
FB2	Address, data, and control output valid	—	13.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	13.7	—	ns	2
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], FB_BE/BWE $\overline{n}$, FB_CS $\overline{n}$, FB_OE, FB_R/W, FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

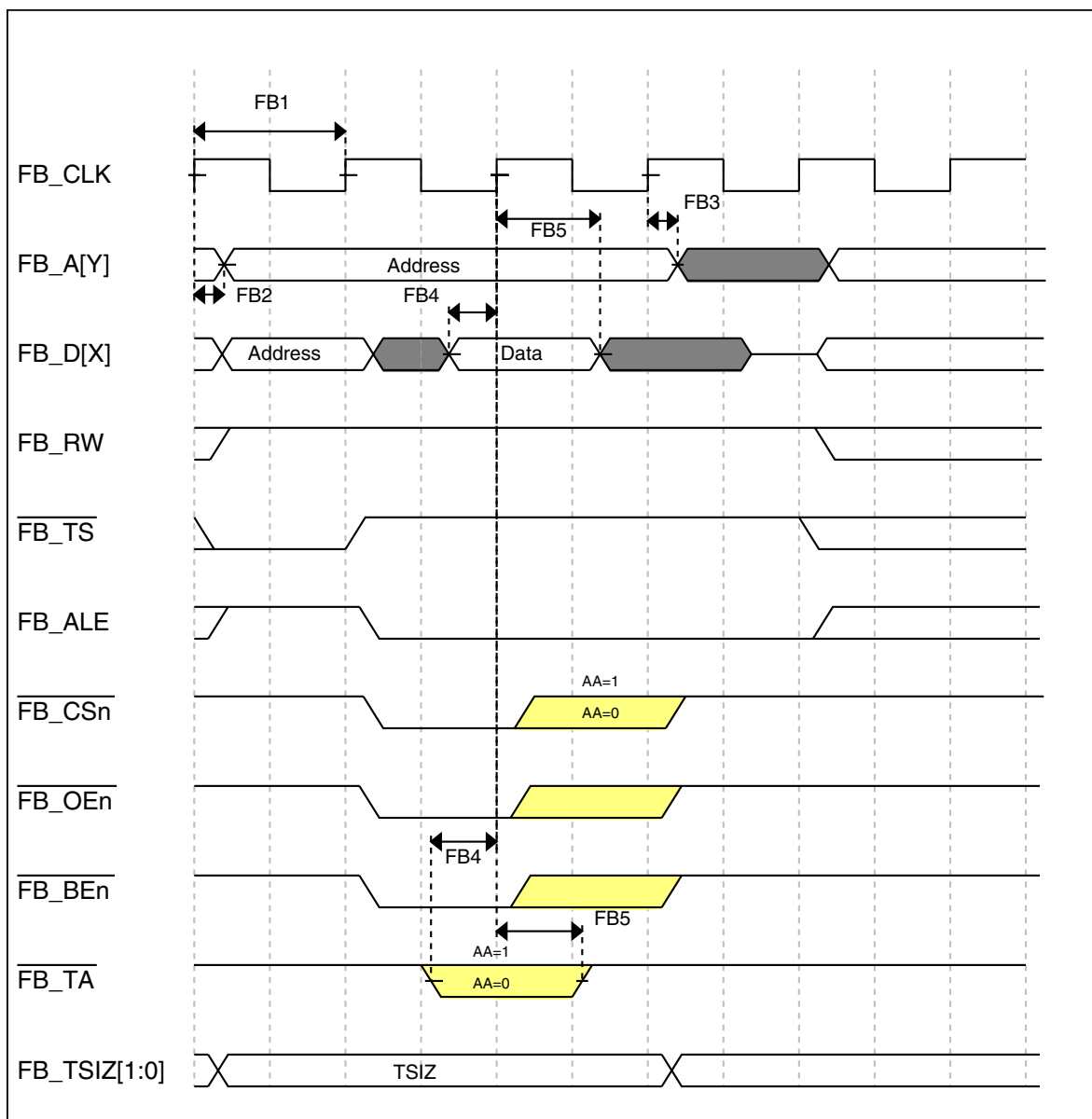


Figure 10. FlexBus read timing diagram

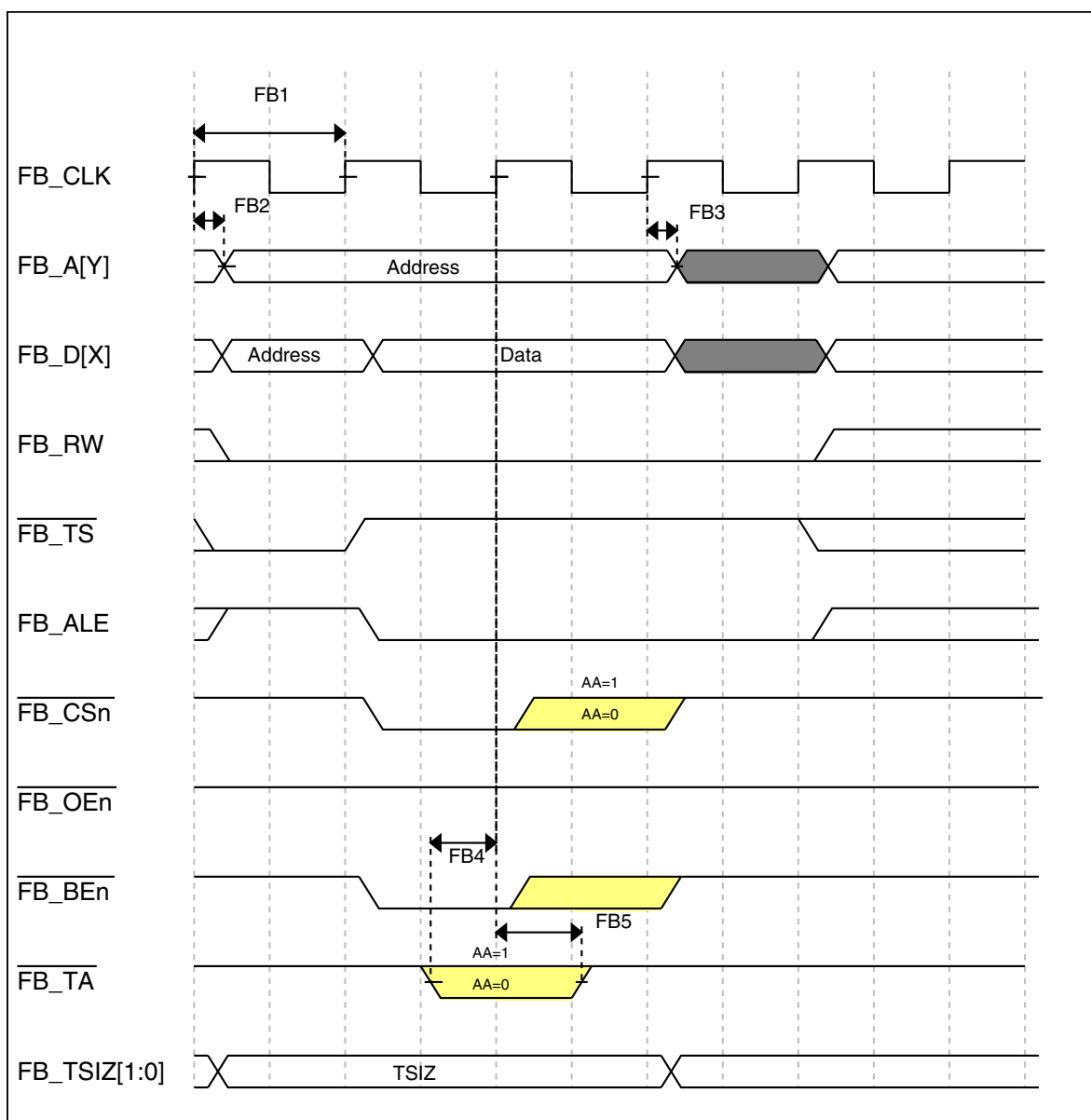


Figure 11. FlexBus write timing diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.6 Analog

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 27](#) and [Table 28](#) are achievable on the differential pins ADCx_DP0, ADCx_DM0, ADCx_DP1, ADCx_DM1, ADCx_DP3, and ADCx_DM3.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in [Table 29](#) and [Table 30](#).

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

6.6.1.1 16-bit ADC operating conditions

Table 27. 16-bit ADC operating conditions

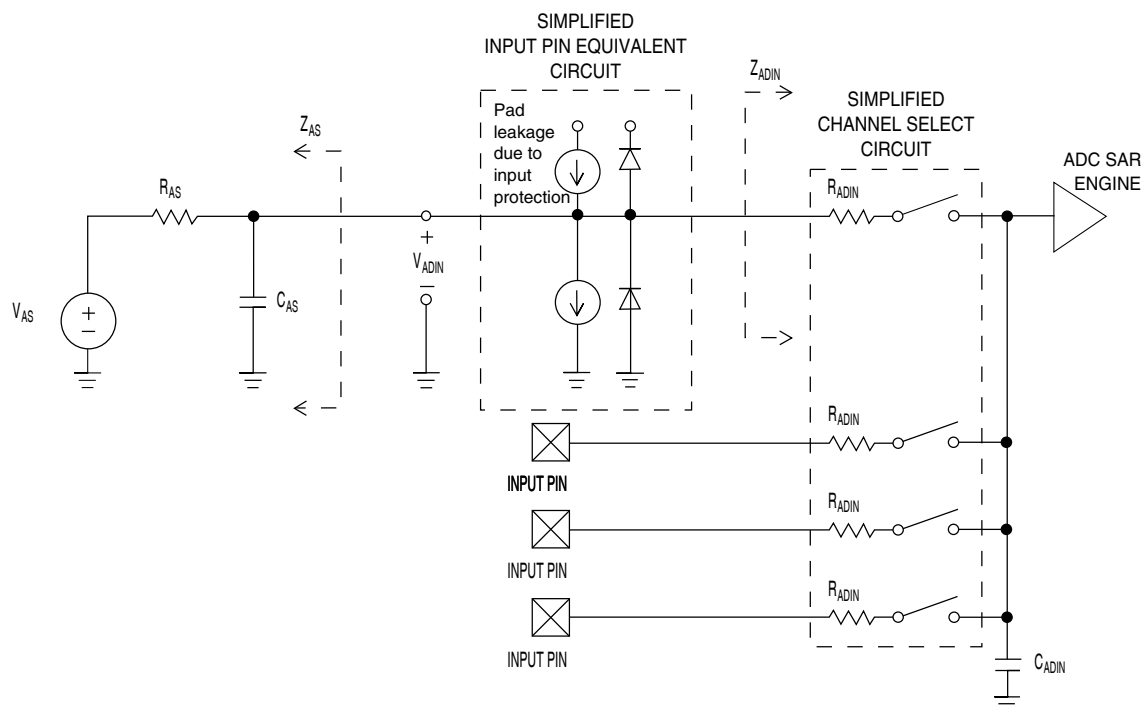
Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV _{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} - V _{DDA})	-100	0	+100	mV	2
ΔV _{SSA}	Ground voltage	Delta to V _{SS} (V _{SS} - V _{SSA})	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	Reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage		V _{REFL}	—	V _{REFH}	V	
C _{ADIN}	Input capacitance	16 bit modes 8/10/12 bit modes	— —	8 4	10 5	pF	
R _{ADIN}	Input resistance		—	2	5	kΩ	
R _{AS}	Analog source resistance	13/12 bit modes f _{ADCK} < 4MHz	—	—	5	kΩ	3
f _{ADCK}	ADC conversion clock frequency	≤ 13 bit modes	1.0	—	18.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16 bit modes	2.0	—	12.0	MHz	5

Table continues on the next page...

Table 27. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C_{rate}	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	6
C_{rate}	ADC conversion rate	16 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	7

1. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25°C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this datasheet were derived from a system which has $<8 \Omega$ analog source resistance. The R_{AS}/C_{AS} time constant should be kept to <1 ns.
4. In order to use the maximum ADC conversion clock frequency ADHSC bit should be set and the ADLPC should be clear.
5. In order to use the maximum ADC conversion clock frequency ADHSC bit should be set and the ADLPC should be clear.
6. For guidelines and examples of conversion rate calculation please download the ADC calculator tool http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fsp=1
7. For guidelines and examples of conversion rate calculation please download the ADC calculator tool http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fsp=1

**Figure 12. ADC input impedance equivalency diagram**

6.6.1.2 16-bit ADC electrical characteristics

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	- ADLPC=1, ADHSC=0 - ADLPC=1, ADHSC=1 - ADLPC=0, ADHSC=0 - ADLPC=0, ADHSC=1	1.2 3.0 2.4 4.4	2.4 4.0 5.2 6.2	3.9 7.3 6.1 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	≤13 bit modes <12 bit modes		±0.8 ±0.5	±TBD ±1	LSB ⁴	ADC conversion clock <12MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
DNL	Differential non-linearity	≤13 bit modes <12 bit modes		±0.7 ±0.2	±TBD ±0.5	LSB ⁴	ADC conversion clock <12MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
INL	Integral non-linearity	≤13 bit modes <12 bit modes	— —	±1.0 ±0.5	±TBD ±TBD	LSB ⁴	Max averaging
E_{FS}	Full-scale error	≤13 bit modes <12 bit modes	— —	±0.4 ±1.0	±TBD ±TBD	LSB ⁴	$V_{ADIN} = V_{DDA}$
E_Q	Quantization error	16 bit modes ≤13 bit modes	— —	-1 to 0 —	— ±0.5	LSB ⁴	
ENOB	Effective number of bits	16 bit differential mode - Avg=32 - Avg=1 16 bit single-ended mode - Avg=32 - Avg=1	TBD TBD TBD TBD	13.6 13.2 TBD TBD	— — — —	bits bits bits bits	5

Table continues on the next page...

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16 bit differential mode • Avg=32	—	−94	TBD	dB	5
		16 bit single-ended mode • Avg=32	—	TBD	TBD	dB	
SFDR	Spurious free dynamic range	16 bit differential mode • Avg=32	TBD	95	—	dB	5
		16 bit single-ended mode • Avg=32	TBD	TBD	—	dB	
E _{IL}	Input leakage error		$I_{in} \times R_{AS}$			mV	I_{in} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	• −40°C to 105°C	—	TBD	—	mV/°C	
V _{TEMP25}	Temp sensor voltage	25°C	—	TBD	—	mV	

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0\text{ V}$, Temp = 25°C, $f_{ADCK} = 2.0\text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.
4. $1\text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. Input data is 1 kHz sine wave.

Figure TBD

Figure 13. Typical TUE vs. ADC conversion rate 12-bit single-ended mode

Figure TBD

Figure 14. Typical ENOB vs. Averaging for 16-bit differential and 16-bit single-ended modes

6.6.1.3 16-bit ADC with PGA operating conditions**Table 29. 16-bit ADC with PGA operating conditions**

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
V _{REFPGA}	PGA ref voltage		VREF_OUT T	VREF_OUT T	VREF_OUT T	V	2, 3
V _{ADIN}	Input voltage		V _{SSA}	—	V _{DDA}	V	
V _{CM}	Input Common Mode range		V _{SSA}	—	V _{DDA}	V	
R _{PGAD}	Differential input impedance	Gain = 1, 2, 4, 8 Gain = 16, 32 Gain = 64	— — —	128 64 32	— — —	kΩ	IN+ to IN- ⁴
R _{AS}	Analog source resistance		—	100	—	Ω	5
T _S	ADC sampling time		1.25	—	—	μs	6
C _{rate}	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	18.484	—	450	Ksps	7
		16 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	37.037	—	250	Ksps	8

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREF_OUT)
3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedance of the driven input is R_{PGAD}/2
5. The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25μs time should be allowed for F_{in}=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

6.6.1.4 16-bit ADC with PGA characteristics

Table 30. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
I _{DDA_PGA}	Supply current	Low power (ADC_PGA[PGALPb]=0)	—	420	TBD	μA	2
I _{DC_PGA}	Input DC current		$\frac{2}{R_{PGAD}} \left(\frac{(V_{REFPGA} \times 0.583) - V_{CM}}{(Gain+1)} \right)$			A	3
		Gain =1, V _{REFPGA} =1.2V, V _{CM} =0.5V	—	1.54	—	μA	
		Gain =64, V _{REFPGA} =1.2V, V _{CM} =0.1V	—	0.57	—	μA	
G	Gain ⁴	- PGAG=0 - PGAG=1 - PGAG=2 - PGAG=3 - PGAG=4 - PGAG=5 - PGAG=6	0.95 1.9 3.8 7.6 15.2 30.0 58.8	1 2 4 8 16 31.6 63.3	1.05 2.1 4.2 8.4 16.6 33.2 67.8		R _{AS} < 100Ω
BW	Input signal bandwidth	16-bit modes < 16-bit modes	—	—	4	kHz	
			—	—	40	kHz	
PSRR	Power supply rejection ratio	Gain=1	TBD	TBD	—	dB	V _{DDA} = 3V ±100mV, f _{VDDA} = 50Hz, 60Hz
CMRR	Common mode rejection ratio	- Gain=1 - Gain=64	TBD	TBD	—	dB	V _{CM} = 500mVpp, f _{VCM} = 50Hz, 100Hz
			TBD	TBD	—	dB	
V _{OFS}	Input offset voltage		—	0.2	TBD	mV	Output offset = V _{OFS} *(Gain+1)
T _{GSW}	Gain switching settling time		—	—	10	μs	5
dG/dT	Gain drift over temperature	- Gain=1 - Gain=64	—	TBD	TBD	ppm/°C	0 to 50°C
			—	TBD	TBD	ppm/°C	
dV _{OFS} /dT	Offset drift over temperature	Gain=1	—	TBD	TBD	ppm/°C	0 to 50°C, ADC Averaging=32
dG/dV _{DDA}	Gain drift over supply voltage	- Gain=1 - Gain=64	—	TBD	TBD	%/V	V _{DDA} from 1.71 to 3.6V
			—	TBD	TBD	%/V	

Table continues on the next page...

Table 30. 16-bit ADC with PGA characteristics (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
E_{IL}	Input leakage error	All modes	$I_{in} \times R_{AS}$			mV	I_{in} = leakage current (refer to the MCU's voltage and current operating ratings)
$V_{PP,DIFF}$	Maximum differential input signal swing		$\left(\frac{(\min(V_X, V_{DDA} - V_X) - 0.2) \times 4}{\text{Gain}} \right)$ where $V_X = V_{REFPGA} \times 0.583$			V	6
SNR	Signal-to-noise ratio	- Gain=1 - Gain=64	TBD	83.0	—	dB	16-bit differential mode, Average=32
			TBD	57.5	—	dB	
THD	Total harmonic distortion	- Gain=1 - Gain=64	TBD	89.4	—	dB	16-bit differential mode, Average=32, $f_{in}=500\text{Hz}$
			TBD	90.0	—	dB	
SFDR	Spurious free dynamic range	- Gain=1 - Gain=64	TBD	90.9	—	dB	16-bit differential mode, Average=32, $f_{in}=500\text{Hz}$
			TBD	77.0	—	dB	
ENOB	Effective number of bits	• Gain=1, Average=4	TBD	12.3	—	bits	16-bit differential mode, $f_{in}=100\text{Hz}$
		• Gain=1, Average=8	TBD	12.7	—	bits	
		• Gain=64, Average=4	TBD	8.4	—	bits	
		• Gain=64, Average=8	TBD	8.7	—	bits	
		• Gain=1, Average=32	TBD	13.3	—	bits	
		• Gain=2, Average=32	TBD	13.1	—	bits	
		• Gain=4, Average=32	TBD	12.5	—	bits	
		• Gain=8, Average=32	TBD	11.8	—	bits	
		• Gain=16, Average=32	TBD	11.1	—	bits	
		• Gain=32, Average=32	TBD	10.2	—	bits	
		• Gain=64, Average=32	TBD	9.3	—	bits	
SINAD	Signal-to-noise plus distortion ratio	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	

1. Typical values assume $V_{DDA}=3.0\text{V}$, $\text{Temp}=25^\circ\text{C}$, $f_{ADCK}=6\text{MHz}$ unless otherwise stated.
2. This current is a PGA module adder, in addition to and ADC conversion currents.
3. Between $IN+$ and $IN-$. The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function of input common mode voltage (V_{CM}) and the PGA gain.
4. $\text{Gain} = 2^{\text{PGAG}}$
5. After changing the PGA gain setting, a minimum of 2 ADC+PGA conversions should be ignored.

6. Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

6.6.2 CMP and 6-bit DAC electrical specifications

Table 31. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μ A
$I_{DDL S}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μ A
V_{AIN}	Analog input voltage	$V_{SS} - 0.3$	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis ¹				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOH}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOI}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	120	250	600	ns
	Analog comparator initialization delay ²	—	—	40	μ s
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μ A
INL	6-bit DAC integral non-linearity	−0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	−0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}-0.6V$.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

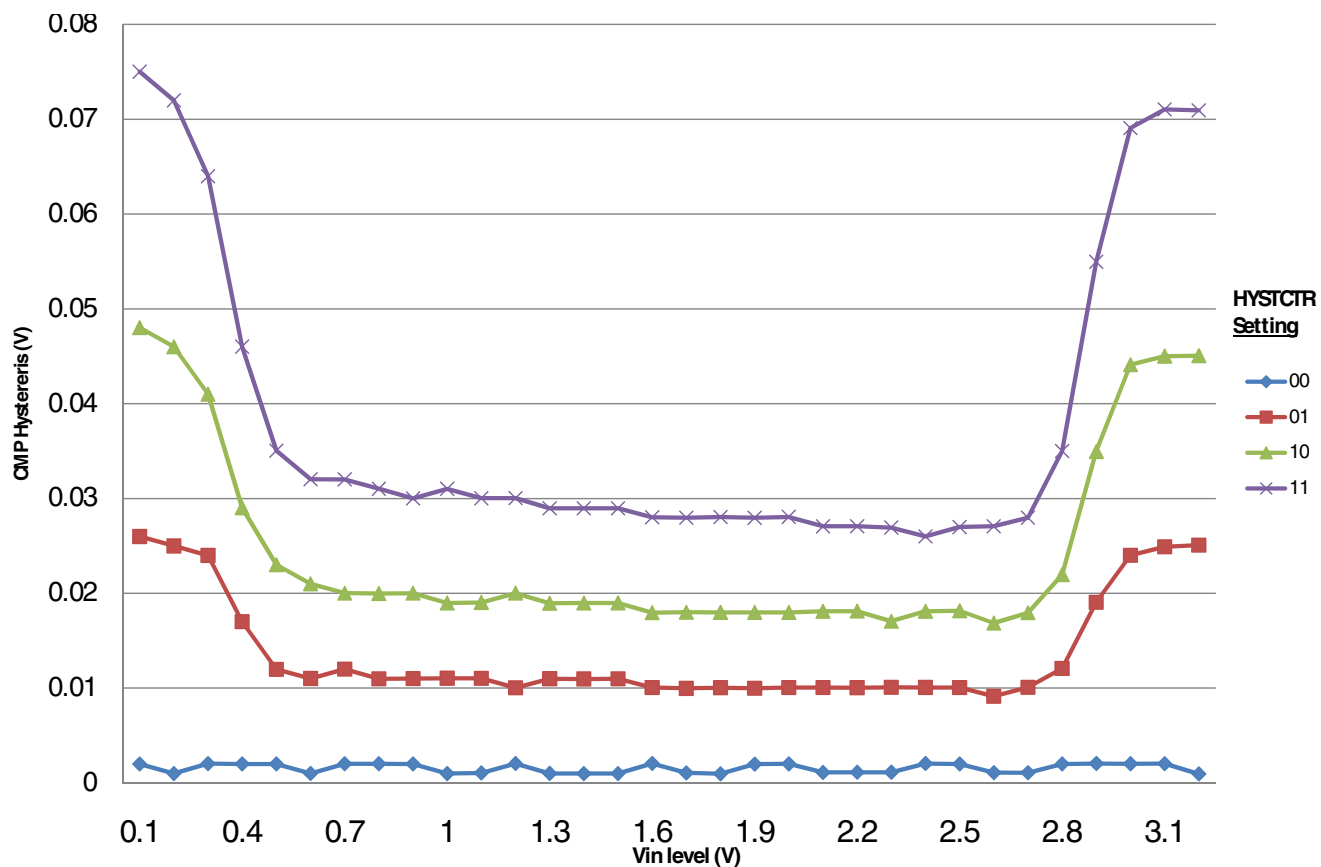


Figure 15. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)

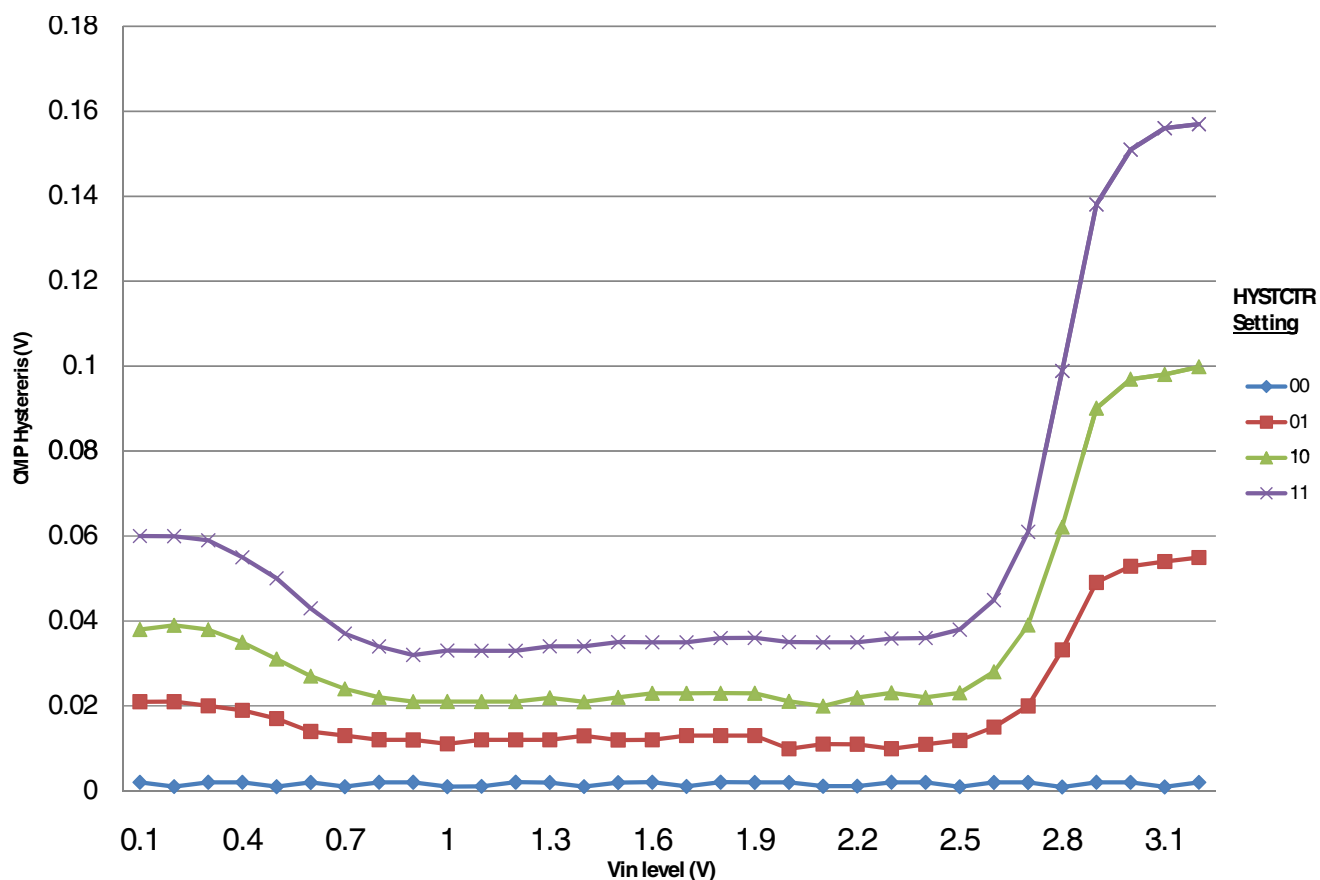


Figure 16. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

6.6.3 12-bit DAC electrical characteristics

6.6.3.1 12-bit DAC operating requirements

Table 32. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
T_A	Temperature	-40	105	°C	
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be VDDA or the voltage output of the VREF module (VREF_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

6.6.3.2 12-bit DAC operating behaviors**Table 33. 12-bit DAC operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF	$V_{DACR} - 100$	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	± 8	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2 V$	—	—	± 1	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$	—	—	± 1	LSB	4
V_{OFFSET}	Offset error	—	± 0.4	± 0.8	%FSR	5
E_G	Gain error	—	± 0.1	± 0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4 V$	60		90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	$\mu V/C$	6
T_{GE}	Temperature coefficient gain error	—	TBD	—	ppm of FSR/C	
A_C	Offset aging coefficient	—	—	TBD	$\mu V/yr$	
R_{op}	Output resistance load = 3 k Ω	—	—	250	Ω	
SR	Slew rate -80h $\rightarrow$ F7Fh $\rightarrow$ 80h • High power (SP_{HP}) • Low power (SP_{LP})	1.2 0.05	1.7 0.12	— —	V/ μs	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth • High power (SP_{HP}) • Low power (SP_{LP})	550 40	— —	— —	kHz	

1. Settling within ± 1 LSB
2. The INL is measured for 0+100mV to $V_{DACR} - 100$ mV
3. The DNL is measured for 0+100 mV to $V_{DACR} - 100$ mV
4. The DNL is measured for 0+100mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4V$
5. Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV

6. VDDA = 3.0V, reference select set for VDDA (DACx_CO:DACRFS = 1), high power mode(DACx_C0:LPEN = 0), DAC set to 0x800, Temp range from -40C to 105C

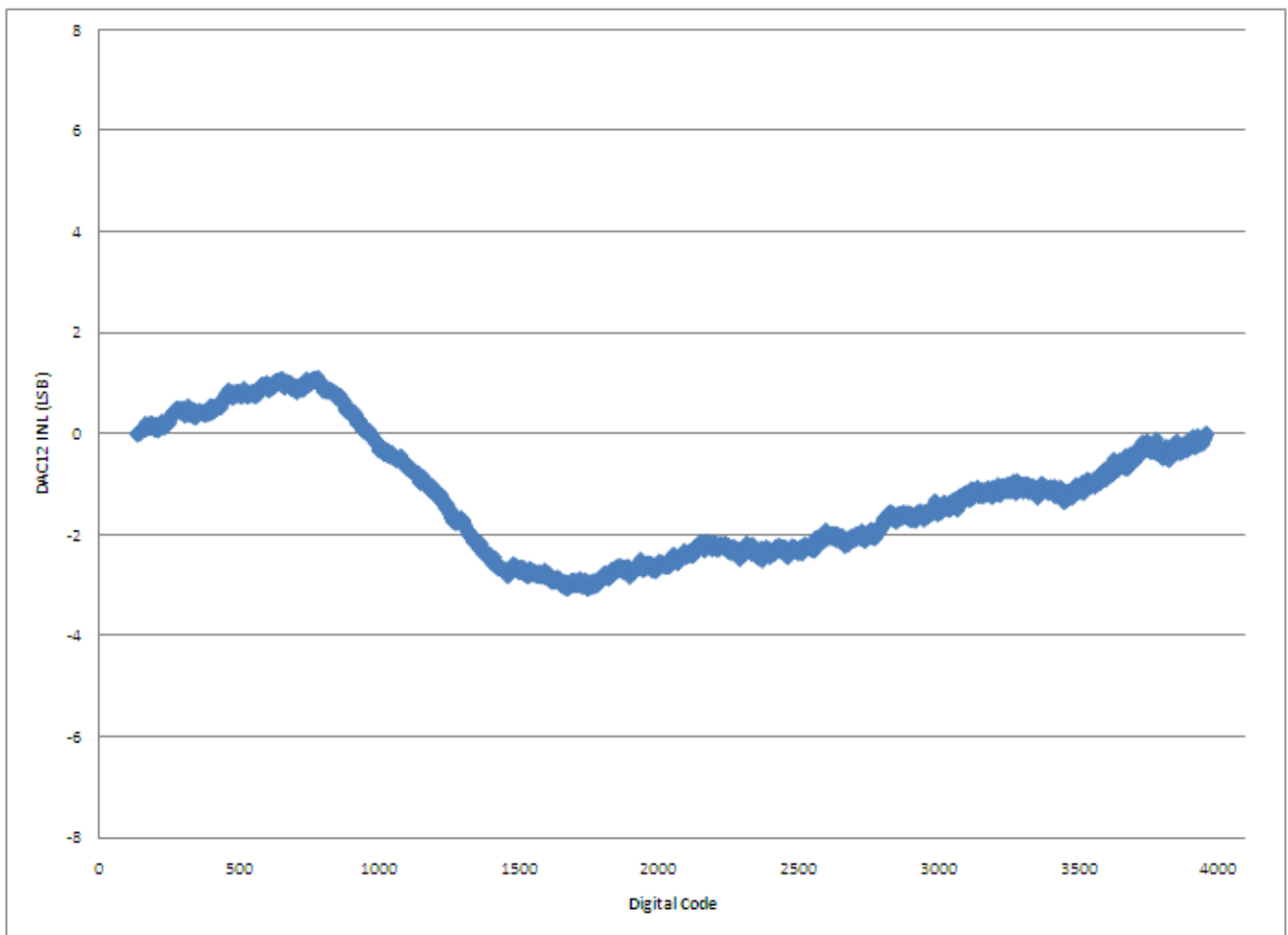


Figure 17. Typical INL error vs. digital code

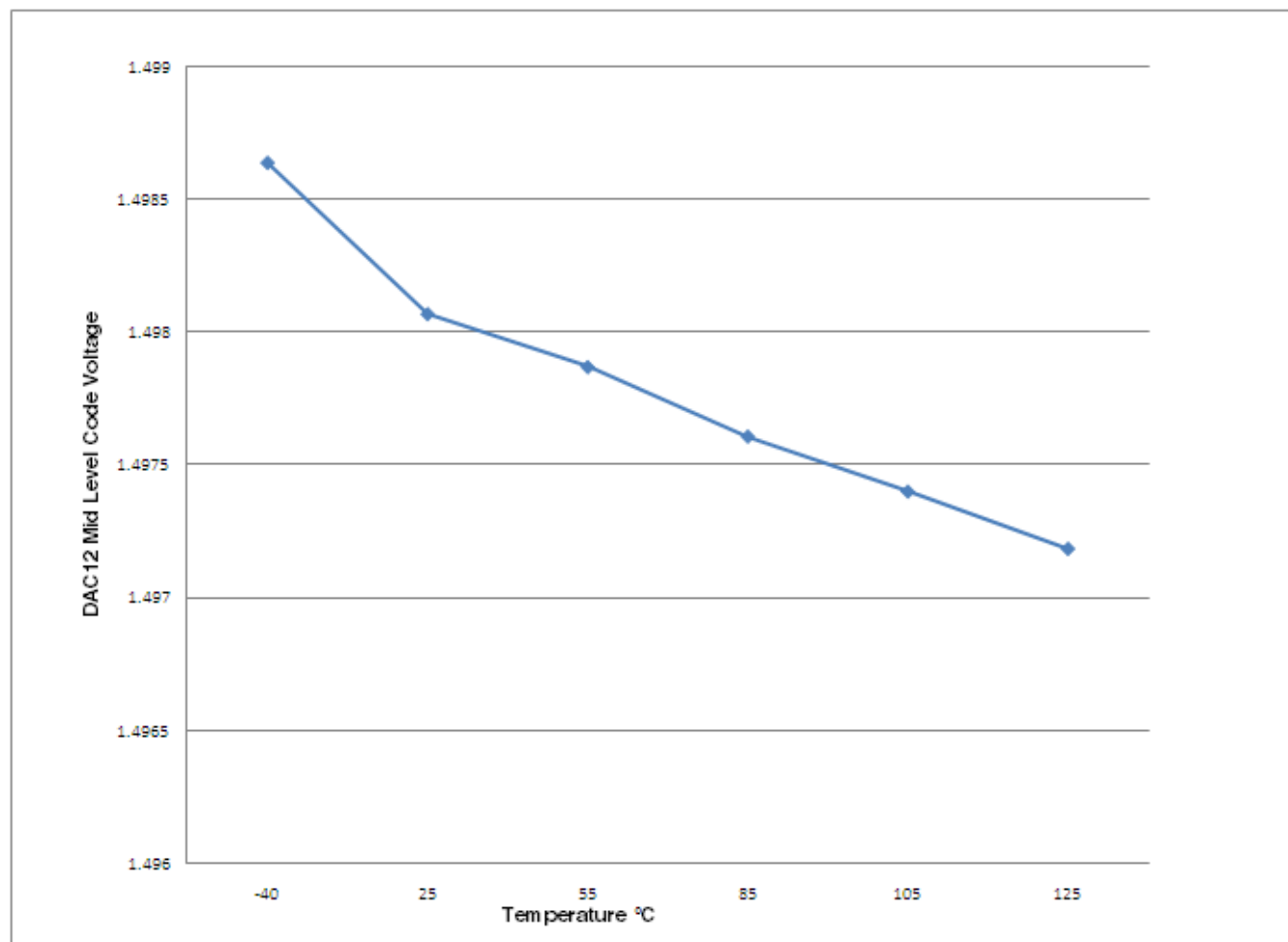


Figure 18. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 34. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	-40	105	°C	
C_L	Output load capacitance	—	100	nF	

Table 35. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25°C	TBD	1.2	TBD	V	

Table continues on the next page...

Table 35. VREF full-range operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with— factory trim	TBD	—	TBD	V	
V_{out}	Voltage reference output — user trim	1.198	—	1.202	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{drift}	Temperature drift ($V_{max} - V_{min}$ across the full temperature range)	—	—	40	mV	See Figure 19
A_c	Aging coefficient	—	—	TBD	ppm/year	
I_{bg}	Bandgap only (MODE_LV = 00) current	—	—	TBD	μA	
I_{tr}	Tight-regulation buffer (MODE_LV = 10) current	—	—	1.1	mA	
ΔV_{LOAD}	Load regulation (MODE_LV = 10) • current = + 1.0 mA • current = - 1.0 mA	—	—	TBD	mV	1
		—	—	TBD		
T_{stup}	Buffer startup time	—	—	100	μs	
DC	Line regulation (power supply rejection)	—	—	TBD	mV	
		-60	—	TBD	dB	

1. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 36. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	$^{\circ}C$	

Table 37. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	TBD	TBD	V	

TBD

Figure 19. Typical output vs. temperature

TBD

Figure 20. Typical output vs. VDD

6.7 Timers

See [General switching specifications](#).

6.8 Communication interfaces

6.8.1 CAN switching specifications

See [General switching specifications](#).

6.8.2 DSPI switching specifications (low-speed mode)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 38. Master mode DSPI timing (low-speed mode)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns	
DS3	DSPI_PCS n valid to DSPI_SCK delay	$(t_{\text{BUS}} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCS n invalid delay	$(t_{\text{BUS}} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

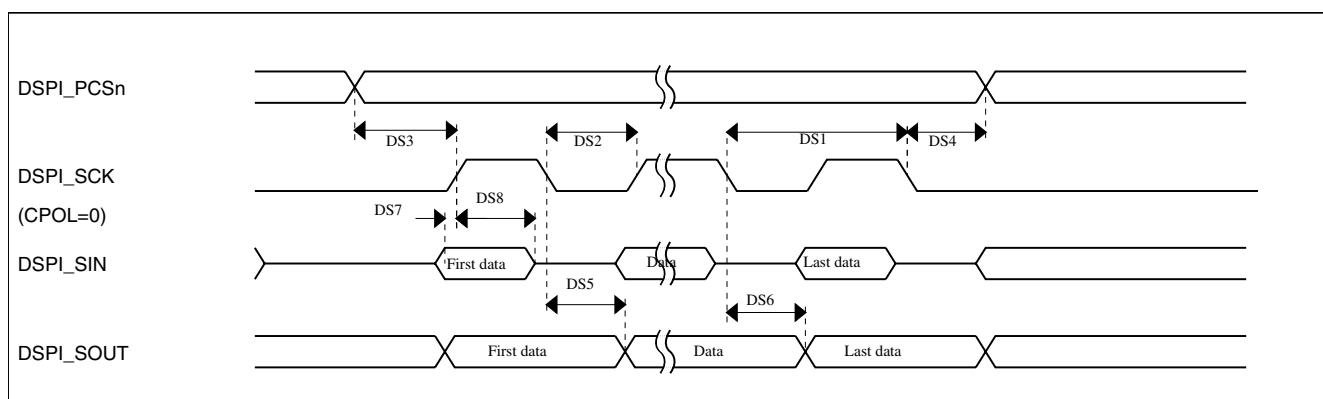


Figure 21. DSPI classic SPI timing — master mode

Table 39. Slave mode DSPI timing (low-speed mode)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SS to DSPI_SCK input setup	5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	15	—	ns
DS15	$\overline{DSPI_SS}$ active to DSPI_SOUT driven	—	19	ns
DS16	$\overline{DSPI_SS}$ inactive to DSPI_SOUT not driven	—	19	ns

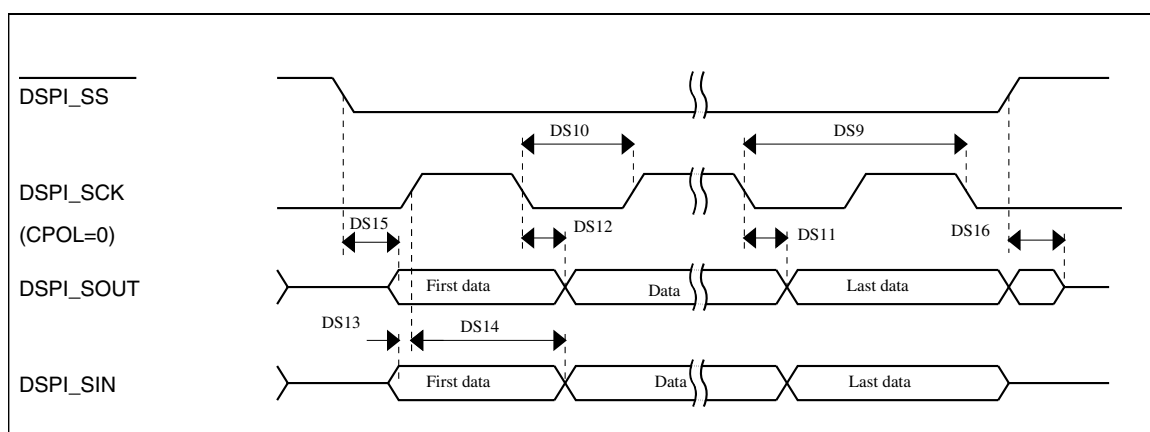


Figure 22. DSPI classic SPI timing — slave mode

6.8.3 DSPI switching specifications (high-speed mode)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 40. Master mode DSPI timing (high-speed mode)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns	
DS3	DSPI_PCS $_n$ valid to DSPI_SCK delay	$(t_{\text{BUS}} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCS $_n$ invalid delay	$(t_{\text{BUS}} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	TBD	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

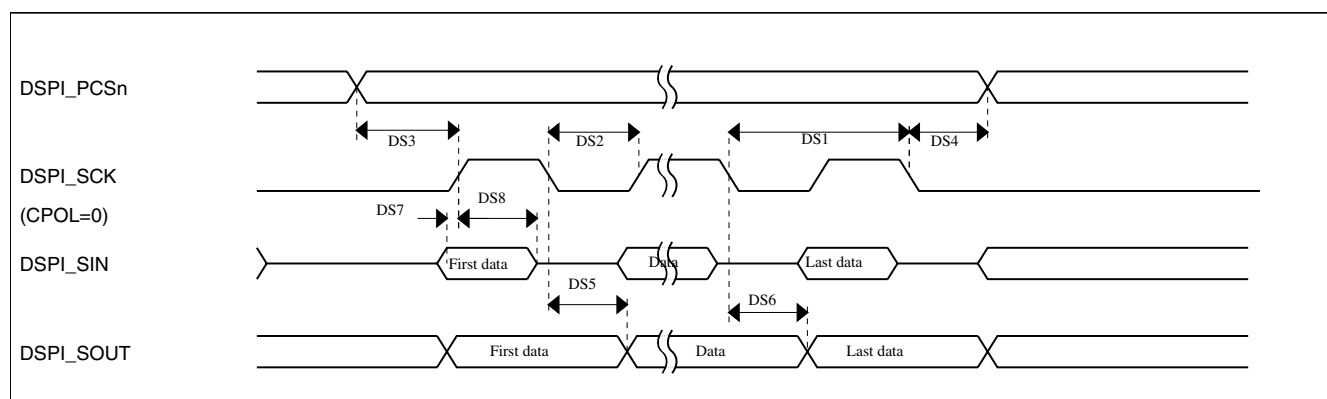


Figure 23. DSPI classic SPI timing — master mode

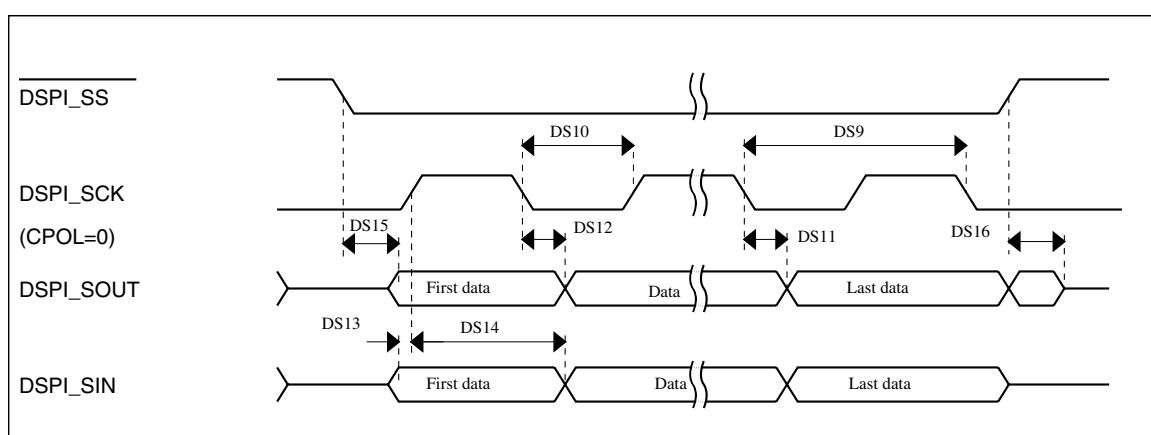
Table 41. Slave mode DSPI timing (high-speed mode)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz

Table continues on the next page...

Table 41. Slave mode DSPI timing (high-speed mode) (continued)

Num	Description	Min.	Max.	Unit
DS9	DSPI_SCK input cycle time	$4 \times t_{\text{BUS}}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

**Figure 24. DSPI classic SPI timing — slave mode**

6.8.4 I²C switching specifications

See [General switching specifications](#).

6.8.5 UART switching specifications

See [General switching specifications](#).

6.8.6 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 42. SDHC switching specifications

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
Card input clock				
f _{pp}	Clock frequency (low speed)	0	400	kHz
f _{pp}	Clock frequency (SD\SDIO full speed)	0	25	MHz
f _{pp}	Clock frequency (MMC full speed)	0	20	MHz
f _{OD}	Clock frequency (identification mode)	0	400	kHz
t _{WL}	Clock low time	7	—	ns
t _{WH}	Clock high time	7	—	ns
t _{TLH}	Clock rise time	—	3	ns
t _{THL}	Clock fall time	—	3	ns
SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
t _{OD}	SDHC output delay (output valid)	-5	6.5	ns
SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
t _{THL}	SDHC input setup time	5	—	ns
t _{THL}	SDHC input hold time	0	—	ns

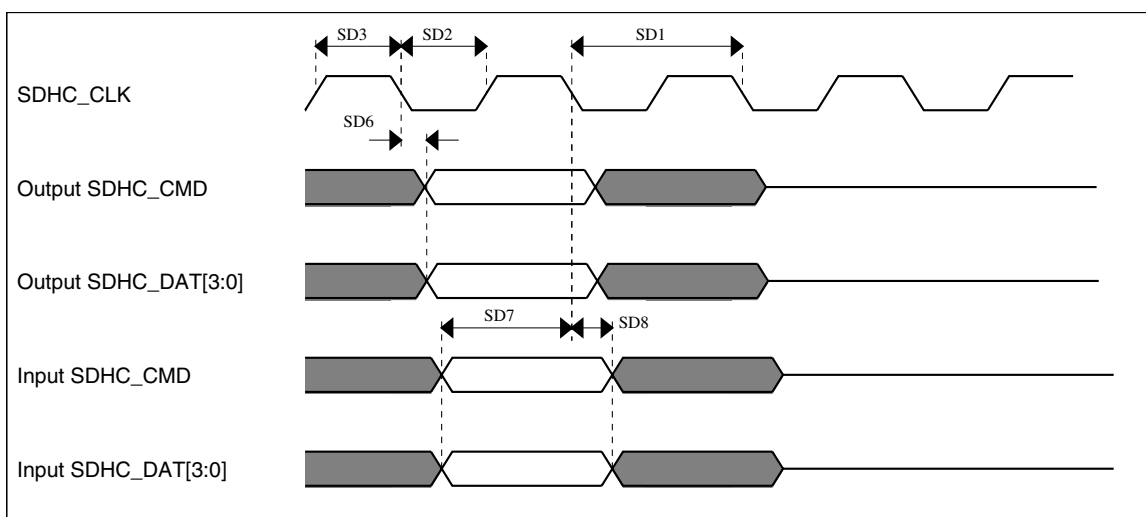


Figure 25. SDHC timing

6.8.7 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 43. I²S master mode timing

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	$2 \times t_{SYS}$		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	$5 \times t_{SYS}$	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	-2.5	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	-3	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	20	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

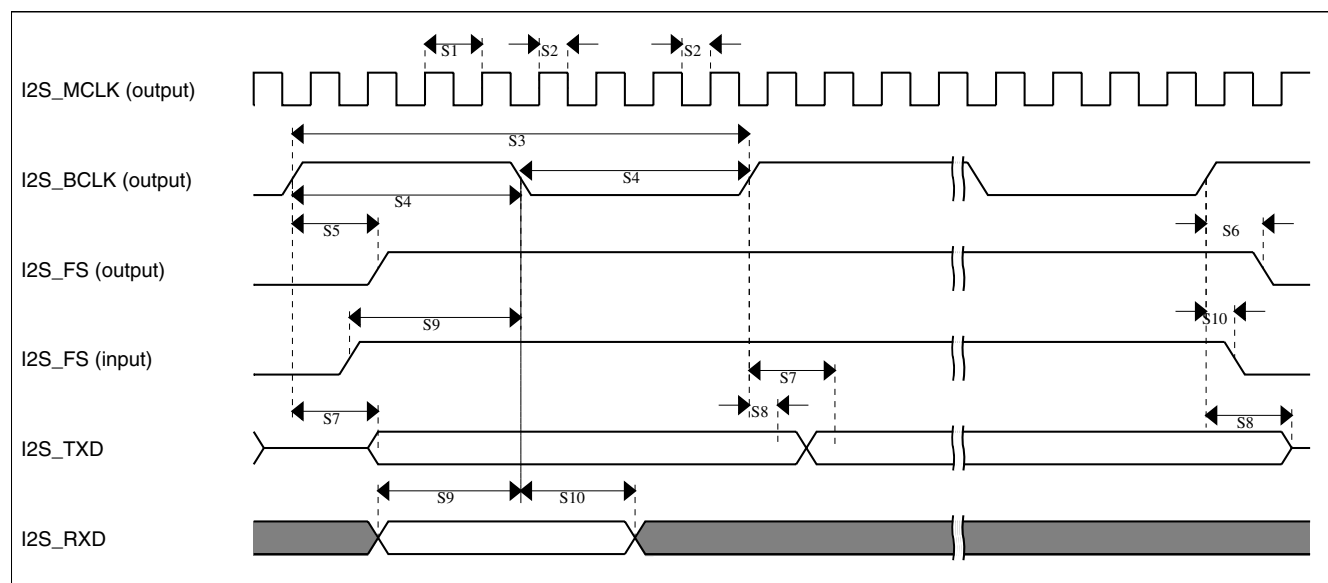
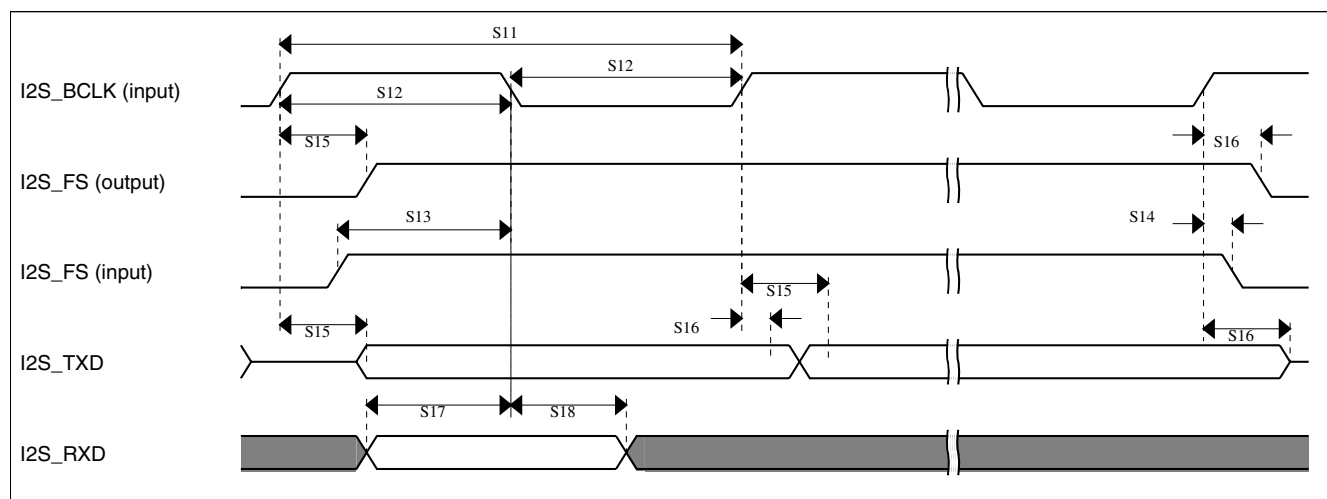


Figure 26. I²S timing — master mode

Table 44. I²S slave mode timing

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_BCLK cycle time (input)	8 x t _{sys}	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	10	—	ns
S14	I2S_FS input hold after I2S_BCLK	3	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	20	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns

**Figure 27. I²S timing — slave modes**

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 45. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{DDTSI}	Operating voltage	1.71	—	3.6	V	
C _{ELE}	Target electrode capacitance range	1	20	500	pF	1
f _{REFmax}	Reference oscillator frequency	—	5.5	TBD	MHz	2
f _{ELEmax}	Electrode oscillator frequency	—	0.5	TBD	MHz	3

Table continues on the next page...

Table 45. TSI electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
C _{REF}	Internal reference capacitor	TBD	1	TBD	pF	
V _{DELTA}	Oscillator delta voltage	TBD	600	TBD	mV	4
I _{REF}	Reference oscillator current source base current	—	1.133	TBD	μA	3, 5
I _{ELE}	Electrode oscillator current source base current	—	1.133	TBD	μA	3, 5
Pres5	Electrode capacitance measurement precision	—	TBD	TBD	%	6
Pres20	Electrode capacitance measurement precision	—	TBD	TBD	%	7
Pres100	Electrode capacitance measurement precision	—	TBD	TBD	%	8
MaxSens20	Maximum sensitivity @ 20 pF electrode	0.003	0.25	—	fF/count	9
MaxSens	Maximum sensitivity	0.003	—	—	fF/count	10
Res	Resolution	—	—	16	bits	
T _{Con20}	Response time @ 20 pF	8	15	25	μs	11
I _{TSI_RUN}	Current added in run mode	—	55	—	μA	
I _{TSI_LP}	Low power mode current adder	—	1.3	TBD	μA	12

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. CAPTRM=7, DELVOL=7, and fixed external capacitance of 20 pF.
3. CAPTRM=0, DELVOL=2, and fixed external capacitance of 20 pF.
4. CAPTRM=0, EXTCHRG=9, and fixed external capacitance of 20 pF.
5. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
6. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; lext = 16.
7. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; lext = 16.
8. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; lext = 16.
9. Measured with a 20 pF electrode, reference oscillator frequency of ~5 MHz (I_{REF} = 5 μA, REFCHRG = 4), PS = 128, NSCN = 2; lext = 16 (EXTCHRG = 15).
10. Typical value depends on the configuration used.
11. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, DELVOL = 2, EXTCHRG = 15.
12. CAPTRM=7, DELVOL=2, REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to <http://www.freescale.com> and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
144-pin LQFP	98ASS23177W
144-pin MAPBGA	98ASA00222D

8 Pinout

8.1 K10 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

144 LQFP	144 MAPBGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
—	L5	RESERVED	RESERVED	RESERVED								
—	M5	NC	NC	NC								
—	A10	NC	NC	NC								
—	B10	NC	NC	NC								
—	C10	NC	NC	NC								
1	D3	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1		I2C1_SDA		
2	D2	PTE1	ADC1_SE5a	ADC1_SE5a	PTE1	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C1_SCL		
3	D1	PTE2	ADC1_SE6a	ADC1_SE6a	PTE2	SPI1_SCK	UART1_CTS_b	SDHC0_DCLK				
4	E4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_b	SDHC0_CMD				
5	E5	VDD	VDD	VDD								
6	F6	VSS	VSS	VSS								
7	E3	PTE4	DISABLED		PTE4	SPI1_PCS0	UART3_TX	SDHC0_D3				
8	E2	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2				
9	E1	PTE6	DISABLED		PTE6	SPI1_PCS3	UART3_CTS_b	I2S0_MCLK		I2S0_CLKIN		
10	F4	PTE7	DISABLED		PTE7		UART3_RTS_b	I2S0_RXD				
11	F3	PTE8	DISABLED		PTE8		UART5_TX	I2S0_RX_FS				
12	F2	PTE9	DISABLED		PTE9		UART5_RX	I2S0_RX_BCLK				
13	F1	PTE10	DISABLED		PTE10		UART5_CTS_b	I2S0_TXD				

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
14	G4	PTE11	DISABLED		PTE11		UART5_RT S_b	I2S0_TX_F S				
15	G3	PTE12	DISABLED		PTE12			I2S0_TX_B CLK				
16	E6	VDD	VDD	VDD								
17	F7	VSS	VSS	VSS								
18	H1	PTE16	ADC0_SE4 a	ADC0_SE4 a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN 0		FTM0_FLT3		
19	H2	PTE17	ADC0_SE5 a	ADC0_SE5 a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN 1		LPT0_ALT3		
20	G1	PTE18	ADC0_SE6 a	ADC0_SE6 a	PTE18	SPI0_SOUT	UART2_CT S_b	I2C0_SDA				
21	G2	PTE19	ADC0_SE7 a	ADC0_SE7 a	PTE19	SPI0_SIN	UART2_RT S_b	I2C0_SCL				
22	H3	VSS	VSS	VSS								
23	J1	ADC0_DP1	ADC0_DP1	ADC0_DP1								
24	J2	ADC0_DM1	ADC0_DM1	ADC0_DM1								
25	K1	ADC1_DP1	ADC1_DP1	ADC1_DP1								
26	K2	ADC1_DM1	ADC1_DM1	ADC1_DM1								
27	L1	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3								
28	L2	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								
29	M1	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
30	M2	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
31	H5	VDDA	VDDA	VDDA								
32	G5	VREFH	VREFH	VREFH								
33	G6	VREFL	VREFL	VREFL								
34	H6	VSSA	VSSA	VSSA								
35	K3	ADC1_SE1 6/ CMP2_IN2/ ADC0_SE2 2	ADC1_SE1 6/ CMP2_IN2/ ADC0_SE2 2	ADC1_SE1 6/ CMP2_IN2/ ADC0_SE2 2								
36	J3	ADC0_SE1 6/ CMP1_IN2/ ADC0_SE2 1	ADC0_SE1 6/ CMP1_IN2/ ADC0_SE2 1	ADC0_SE1 6/ CMP1_IN2/ ADC0_SE2 1								
37	M3	VREF_OUT/ CMP1_IN5/	VREF_OUT/ CMP1_IN5/	VREF_OUT/ CMP1_IN5/								

Pinout

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
		CMP0_IN5/ ADC1_SE1 8	CMP0_IN5/ ADC1_SE1 8	CMP0_IN5/ ADC1_SE1 8								
38	L3	DAC0_OUT/ CMP1_IN3/ ADC0_SE2 3	DAC0_OUT/ CMP1_IN3/ ADC0_SE2 3	DAC0_OUT/ CMP1_IN3/ ADC0_SE2 3								
39	L4	DAC1_OUT/ CMP2_IN3/ ADC1_SE2 3	DAC1_OUT/ CMP2_IN3/ ADC1_SE2 3	DAC1_OUT/ CMP2_IN3/ ADC1_SE2 3								
40	M7	XTAL32	XTAL32	XTAL32								
41	M6	EXTAL32	EXTAL32	EXTAL32								
42	L6	VBAT	VBAT	VBAT								
43	—	VDD	VDD	VDD								
44	—	VSS	VSS	VSS								
45	M4	PTE24	ADC0_SE1 7	ADC0_SE1 7	PTE24	CAN1_TX	UART4_TX			EWM_OUT _b		
46	K5	PTE25	ADC0_SE1 8	ADC0_SE1 8	PTE25	CAN1_RX	UART4_RX			EWM_IN		
47	K4	PTE26	DISABLED		PTE26		UART4_CT S_b			RTC_CLKO UT		
48	J4	PTE27	DISABLED		PTE27		UART4_RT S_b					
49	H4	PTE28	DISABLED		PTE28							
50	J5	PTA0	JTAG_TCL K/ SWD_CLK/ EZP_CLK	TSIO_CH1	PTA0	UART0_CT S_b	FTM0_CH5				JTAG_TCL K/ SWD_CLK	EZP_CLK
51	J6	PTA1	JTAG_TDI/ EZP_DI	TSIO_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
52	K6	PTA2	JTAG_TDO/ TRACE_SW O/EZP_DO	TSIO_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SW O	EZP_DO
53	K7	PTA3	JTAG_TMS/ SWD_DIO	TSIO_CH4	PTA3	UART0_RT S_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
54	L7	PTA4	NMI_b/ EZP_CS_b	TSIO_CH5	PTA4		FTM0_CH1				NMI_b	EZP_CS_b
55	M8	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT	I2S0_RX_B CLK	JTAG_TRS T	
56	E7	VDD	VDD	VDD								
57	G7	VSS	VSS	VSS								
58	J7	PTA6	DISABLED		PTA6		FTM0_CH3				TRACE_CL KOUT	
59	J8	PTA7	ADC0_SE1 0	ADC0_SE1 0	PTA7		FTM0_CH4				TRACE_D3	

144 LQF P	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
60	K8	PTA8	ADC0_SE1 1	ADC0_SE1 1	PTA8		FTM1_CH0			FTM1_QD_ PHA	TRACE_D2	
61	L8	PTA9	DISABLED		PTA9		FTM1_CH1			FTM1_QD_ PHB	TRACE_D1	
62	M9	PTA10	DISABLED		PTA10		FTM2_CH0			FTM2_QD_ PHA	TRACE_D0	
63	L9	PTA11	DISABLED		PTA11		FTM2_CH1			FTM2_QD_ PHB		
64	K9	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0			I2S0_TXD	FTM1_QD_ PHA	
65	J9	PTA13	CMP2_IN1	CMP2_IN1	PTA13	CAN0_RX	FTM1_CH1			I2S0_TX_F S	FTM1_QD_ PHB	
66	L10	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_TX_B CLK		
67	L11	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD		
68	K10	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CT S_b			I2S0_RX_F S		
69	K11	PTA17	ADC1_SE1 7	ADC1_SE1 7	PTA17	SPI0_SIN	UART0_RT S_b			I2S0_MCLK	I2S0_CLKIN	
70	E8	VDD	VDD	VDD								
71	G8	VSS	VSS	VSS								
72	M12	PTA18	EXTAL	EXTAL	PTA18		FTM0_FLT2	FTM_CLKIN 0				
73	M11	PTA19	XTAL	XTAL	PTA19		FTM1_FLT0	FTM_CLKIN 1		LPT0_ALT1		
74	L12	RESET_b	RESET_b	RESET_b								
75	K12	PTA24	DISABLED		PTA24					FB_A29		
76	J12	PTA25	DISABLED		PTA25					FB_A28		
77	J11	PTA26	DISABLED		PTA26					FB_A27		
78	J10	PTA27	DISABLED		PTA27					FB_A26		
79	H12	PTA28	DISABLED		PTA28					FB_A25		
80	H11	PTA29	DISABLED		PTA29					FB_A24		
81	H10	PTB0	/ ADC0_SE8/ ADC1_SE8/ TSI0_CH0	/ ADC0_SE8/ ADC1_SE8/ TSI0_CH0	PTB0	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA		
82	H9	PTB1	/ ADC0_SE9/ ADC1_SE9/ TSI0_CH6	/ ADC0_SE9/ ADC1_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_ PHB		
83	G12	PTB2	/ ADC0_SE1 2/TSI0_CH7	/ ADC0_SE1 2/TSI0_CH7	PTB2	I2C0_SCL	UART0_RT S_b			FTM0_FLT3		
84	G11	PTB3	/ ADC0_SE1 3/TSI0_CH8	/ ADC0_SE1 3/TSI0_CH8	PTB3	I2C0_SDA	UART0_CT S_b			FTM0_FLT0		

Pinout

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
85	G10	PTB4	/ ADC1_SE10	/ ADC1_SE10	PTB4					FTM1_FLT0		
86	G9	PTB5	/ ADC1_SE11	/ ADC1_SE11	PTB5					FTM2_FLT0		
87	F12	PTB6	/ ADC1_SE12	/ ADC1_SE12	PTB6				FB_AD23			
88	F11	PTB7	/ ADC1_SE13	/ ADC1_SE13	PTB7				FB_AD22			
89	F10	PTB8			PTB8		UART3_RTS_b		FB_AD21			
90	F9	PTB9			PTB9	SPI1_PCS1	UART3_CTS_b		FB_AD20			
91	E12	PTB10	/ ADC1_SE14	/ ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX		FB_AD19	FTM0_FLT1		
92	E11	PTB11	/ ADC1_SE15	/ ADC1_SE15	PTB11	SPI1_SCK	UART3_TX		FB_AD18	FTM0_FLT2		
93	H7	VSS	VSS	VSS								
94	F5	VDD	VDD	VDD								
95	E10	PTB16	/TSIO_CH9	/TSIO_CH9	PTB16	SPI1_SOUT	UART0_RX		FB_AD17	EWM_IN		
96	E9	PTB17	/TSIO_CH10	/TSIO_CH10	PTB17	SPI1_SIN	UART0_TX		FB_AD16	EWM_OUT_b		
97	D12	PTB18	/TSIO_CH11	/TSIO_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_B CLK	FB_AD15	FTM2_QD_PHA		
98	D11	PTB19	/TSIO_CH12	/TSIO_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_PHB		
99	D10	PTB20			PTB20	SPI2_PCS0			FB_AD31	CMP0_OUT		
100	D9	PTB21			PTB21	SPI2_SCK			FB_AD30	CMP1_OUT		
101	C12	PTB22			PTB22	SPI2_SOUT			FB_AD29	CMP2_OUT		
102	C11	PTB23			PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28			
103	B12	PTC0	/ ADC0_SE14/ TSIO_CH13	/ ADC0_SE14/ TSIO_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG	I2S0_TXD	FB_AD14			
104	B11	PTC1	/ ADC0_SE15/ TSIO_CH14	/ ADC0_SE15/ TSIO_CH14	PTC1	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FB_AD13			
105	A12	PTC2	/ ADC0_SE4b/ CMP1_IN0/ TSIO_CH15	/ ADC0_SE4b/ CMP1_IN0/ TSIO_CH15	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FB_AD12			

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
106	A11	PTC3	/CMP1_IN1	/CMP1_IN1	PTC3	SPI0_PCS1	UART1_RX	FTM0_CH2	FB_CLKOUT			
107	H8	VSS	VSS	VSS								
108	—	VDD	VDD	VDD								
109	A9	PTC4			PTC4	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT		
110	D8	PTC5			PTC5	SPI0_SCK		LPT0_ALT2	FB_AD10	CMP0_OUT		
111	C8	PTC6	/CMP0_IN0	/CMP0_IN0	PTC6	SPI0_SOUT	PDB0_EXT RG		FB_AD9			
112	B8	PTC7	/CMP0_IN1	/CMP0_IN1	PTC7	SPI0_SIN			FB_AD8			
113	A8	PTC8	/ADC1_SE4 b/ CMP0_IN2	/ADC1_SE4 b/ CMP0_IN2	PTC8		I2S0_MCLK	I2S0_CLKIN	FB_AD7			
114	D7	PTC9	/ADC1_SE5 b/ CMP0_IN3	/ADC1_SE5 b/ CMP0_IN3	PTC9			I2S0_RX_B CLK	FB_AD6	FTM2_FLT0		
115	C7	PTC10	/ADC1_SE6 b/ CMP0_IN4	/ADC1_SE6 b/ CMP0_IN4	PTC10	I2C1_SCL		I2S0_RX_F S	FB_AD5			
116	B7	PTC11	/ADC1_SE7 b	/ADC1_SE7 b	PTC11	I2C1_SDA		I2S0_RXD	FB_RW_b			
117	A7	PTC12			PTC12		UART4_RT S_b		FB_AD27			
118	D6	PTC13			PTC13		UART4_CT S_b		FB_AD26			
119	C6	PTC14			PTC14		UART4_RX		FB_AD25			
120	B6	PTC15			PTC15		UART4_TX		FB_AD24			
121	—	VSS	VSS	VSS								
122	—	VDD	VDD	VDD								
123	A6	PTC16			PTC16	CAN1_RX	UART3_RX		FB_CS5_b/ FB_TSIZ1/ FB_BE23_1 6_BLS15_8 _b			
124	D5	PTC17			PTC17	CAN1_TX	UART3_TX		FB_CS4_b/ FB_TSIZ0/ FB_BE31_2 4_BLS7_0 _b			
125	C5	PTC18			PTC18		UART3_RT S_b		FB_TBST_b /FB_CS2_b/ FB_BE15_8 _BLS23_16 _b			

Pinout

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
126	B5	PTC19			PTC19		UART3_CTS_b		FB_CS3_b/ FB_BE7_0_ BLS31_24_ b	FB_TA_b		
127	A5	PTD0			PTD0	SPI0_PCS0	UART2_RTS_b		FB_ALE/ FB_CS1_b/ FB_TS_b			
128	D4	PTD1	/ ADC0_SE5 b	/ ADC0_SE5 b	PTD1	SPI0_SCK	UART2_CTS_b		FB_CS0_b			
129	C4	PTD2			PTD2	SPI0_SOUT	UART2_RX		FB_AD4			
130	B4	PTD3			PTD3	SPI0_SIN	UART2_TX		FB_AD3			
131	A4	PTD4			PTD4	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FB_AD2	EWM_IN		
132	A3	PTD5	/ ADC0_SE6 b	/ ADC0_SE6 b	PTD5	SPI0_PCS2	UART0_CTS_b	FTM0_CH5	FB_AD1	EWM_OUT_b		
133	A2	PTD6	/ ADC0_SE7 b	/ ADC0_SE7 b	PTD6	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0		
134	M10	VSS	VSS	VSS								
135	F8	VDD	VDD	VDD								
136	A1	PTD7			PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		
137	C9	PTD8	DISABLED		PTD8	I2C0_SCL	UART5_RX			FB_A16		
138	B9	PTD9	DISABLED		PTD9	I2C0_SDA	UART5_TX			FB_A17		
139	B3	PTD10	DISABLED		PTD10		UART5_RTS_b			FB_A18		
140	B2	PTD11	DISABLED		PTD11	SPI2_PCS0	UART5_CTS_b	SDHC0_CLKIN		FB_A19		
141	B1	PTD12	DISABLED		PTD12	SPI2_SCK		SDHC0_D4		FB_A20		
142	C3	PTD13	DISABLED		PTD13	SPI2_SOUT		SDHC0_D5		FB_A21		
143	C2	PTD14	DISABLED		PTD14	SPI2_SIN		SDHC0_D6		FB_A22		
144	C1	PTD15	DISABLED		PTD15	SPI2_PCS1		SDHC0_D7		FB_A23		

8.2 K10 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

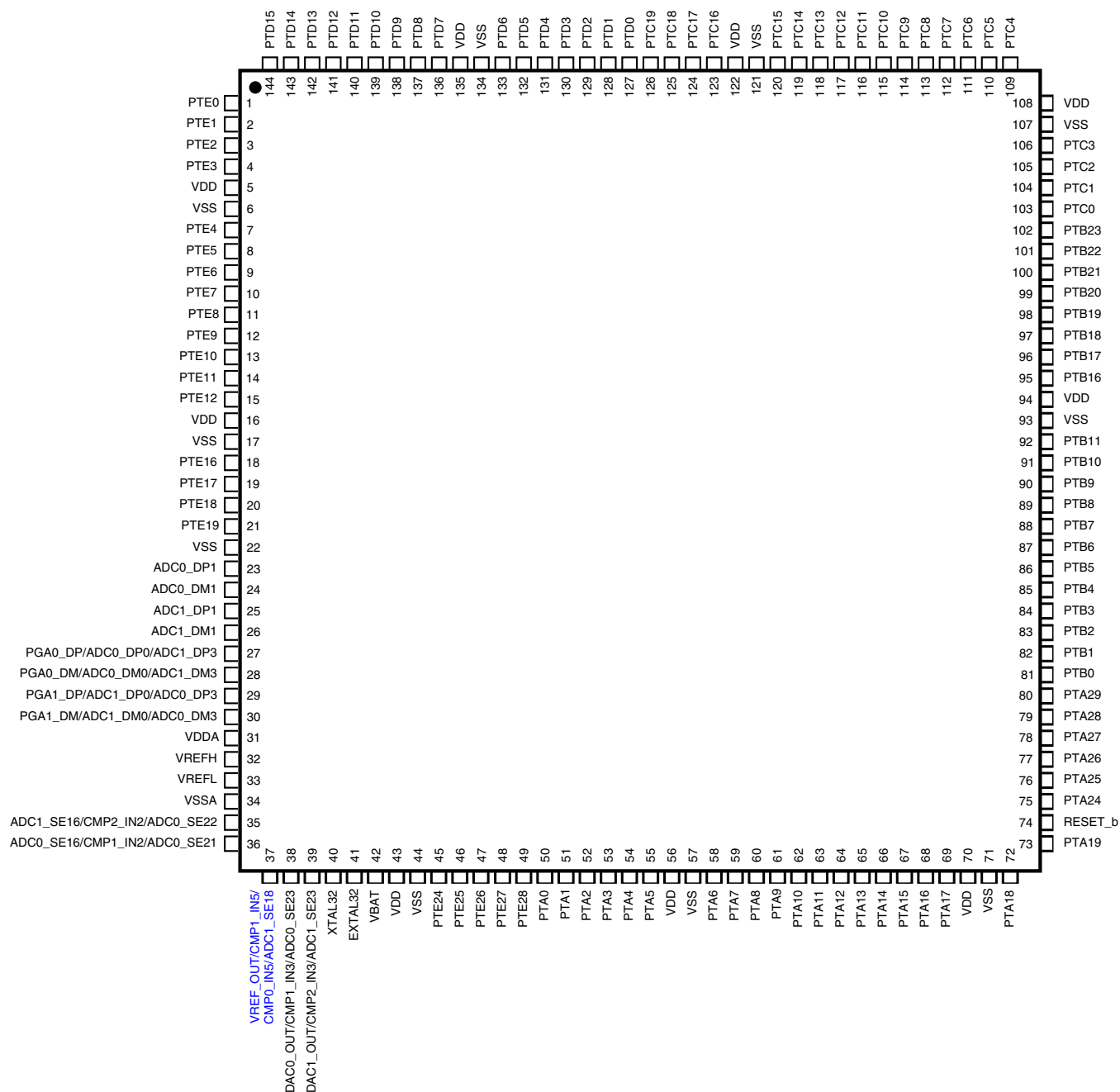


Figure 28. K10 144 LQFP Pinout Diagram

Revision History

	1	2	3	4	5	6	7	8	9	10	11	12	
A	PTD7	PTD6	PTD5	PTD4	PTD0	PTC16	PTC12	PTC8	PTC4	NC	PTC3	PTC2	A
B	PTD12	PTD11	PTD10	PTD3	PTC19	PTC15	PTC11	PTC7	PTD9	NC	PTC1	PTC0	B
C	PTD15	PTD14	PTD13	PTD2	PTC18	PTC14	PTC10	PTC6	PTD8	NC	PTB23	PTB22	C
D	PTE2	PTE1	PTE0	PTD1	PTC17	PTC13	PTC9	PTC5	PTB21	PTB20	PTB19	PTB18	D
E	PTE6	PTE5	PTE4	PTE3	VDD	VDD	VDD	VDD	PTB17	PTB16	PTB11	PTB10	E
F	PTE10	PTE9	PTE8	PTE7	VDD	VSS	VSS	VDD	PTB9	PTB8	PTB7	PTB6	F
G	PTE18	PTE19	PTE12	PTE11	VREFH	VREFL	VSS	VSS	PTB5	PTB4	PTB3	PTB2	G
H	PTE16	PTE17	VSS	PTE28	VDDA	VSSA	VSS	VSS	PTB1	PTB0	PTA29	PTA28	H
J	ADC0_DP1	ADC0_DM1	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	PTE27	PTA0	PTA1	PTA6	PTA7	PTA13	PTA27	PTA26	PTA25	J
K	ADC1_DP1	ADC1_DM1	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	PTE26	PTE25	PTA2	PTA3	PTA8	PTA12	PTA16	PTA17	PTA24	K
L	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC1_OUT/ CMP2_IN3/ ADC1_SE23	RESERVED	VBAT	PTA4	PTA9	PTA11	PTA14	PTA15	RESET_b	L
M	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	PTE24	NC	EXTAL32	XTAL32	PTA5	PTA10	VSS	PTA19	PTA18	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 29. K10 144 MAPBGA Pinout Diagram

9 Revision History

The following table provides a revision history for this document.

Table 46. Revision History

Rev. No.	Date	Substantial Changes
1	11/2010	Initial public revision

Table continues on the next page...

Table 46. Revision History (continued)

Rev. No.	Date	Substantial Changes
2	3/2011	Many updates throughout
3	3/2011	Added sections that were inadvertently removed in previous revision
4	3/2011	Reworded I_C footnote in "Voltage and Current Operating Requirements" table. Added paragraph to "Peripheral operating requirements and behaviors" section. Added "JTAG full voltage range electricals" table to the "JTAG electricals" section.
5	6/2011	• Changed supported part numbers per new part number scheme • Changed <i>DC injection current</i> specs in "Voltage and current operating requirements" table • Changed <i>Input leakage current</i> and <i>internal pullup/pulldown resistor</i> specs in "Voltage and current operating behaviors" table • Split <i>Low power stop mode current</i> specs by temperature range in "Power consumption operating behaviors" table • Changed typical I_{DD_VBAT} spec in "Power consumption operating behaviors" table • Added LPTMR clock specs to "Device clock specifications" table • Changed <i>Minimum external reset pulse width</i> in "General switching specifications" table • Changed <i>PLL operating current</i> in "MCG specifications" table • Added footnote to <i>PLL period jitter</i> in "MCG specifications" table • Changed <i>Supply current</i> in "Oscillator DC electrical specifications" table • Changed <i>Crystal startup time</i> in "Oscillator frequency specifications" table • Changed <i>Operating voltage</i> in "EzPort switching specifications" table • Changed title of "FlexBus switching specifications" table and added Output valid and hold specs • Added "FlexBus full range switching specifications" table • Changed <i>ADC asynchronous clock source</i> specs in "16-bit ADC characteristics" table • Changed <i>Gain</i> spec in "16-bit ADC with PGA characteristics" table • Added typical <i>Input DC current</i> to "16-bit ADC with PGA characteristics" table • Changed <i>Input offset voltage</i> and <i>ENOB</i> notes field in "16-bit ADC with PGA characteristics" table • Changed <i>Analog comparator initialization delay</i> in "Comparator and 6-bit DAC electrical specifications" • Changed <i>Code-to-code settling time</i>, <i>DAC output voltage range low</i>, and <i>Temperature coefficient offset voltage</i> in "12-bit DAC operating behaviors" table • Changed <i>Temperature drift</i> and <i>Load regulation</i> in "VREF full-range operating behaviors" table • Changed <i>DSPI_SCK cycle time</i> specs in "DSPI timing" tables • Changed $\overline{DSPI_SS}$ specs in "Slave mode DSPI timing (low-speed mode)" table • Changed <i>DSPI_SCK to DSPI_SOUT valid</i> spec in "Slave mode DSPI timing (high-speed mode)" table • Changed <i>Reference oscillator current source base current</i> spec and added <i>Low-power current adder</i> footer in "TSI electrical specifications" table

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